ENGINEERING DESIGN FOR ELECTRICAL ENGINEERS

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SPECIFICATIONS—TEMPERATURE MONITOR

Measures and displays temperature over range −40 to +120°F
Temperature accuracy within 1°F
Displays most recent 24-hour degree-days over the range 0 to 99
Printout on paper tape:
  time each hour
  most-recent 24-hour degree days
Power supply: 115 V-AC with backup battery for 3 days' data retention
Display: 6 digit, 0.5-in. red LEDs
Keyboard: 36 keys
Printer: Thermal, 5 × 7 matrix characters, prints 20 characters/line
Size: 17 in. wide, 10 in. deep, 2 in. high
Weight: 3 lbs.

WILCOX Engineering	LEWISBURG, PENNSYLVANIA 17837
REVISIONS	TITLE: Temperature Monitor
DRAWN / CHECKED / APPROVED	SCALE / DRAWING NO: 1 of 3

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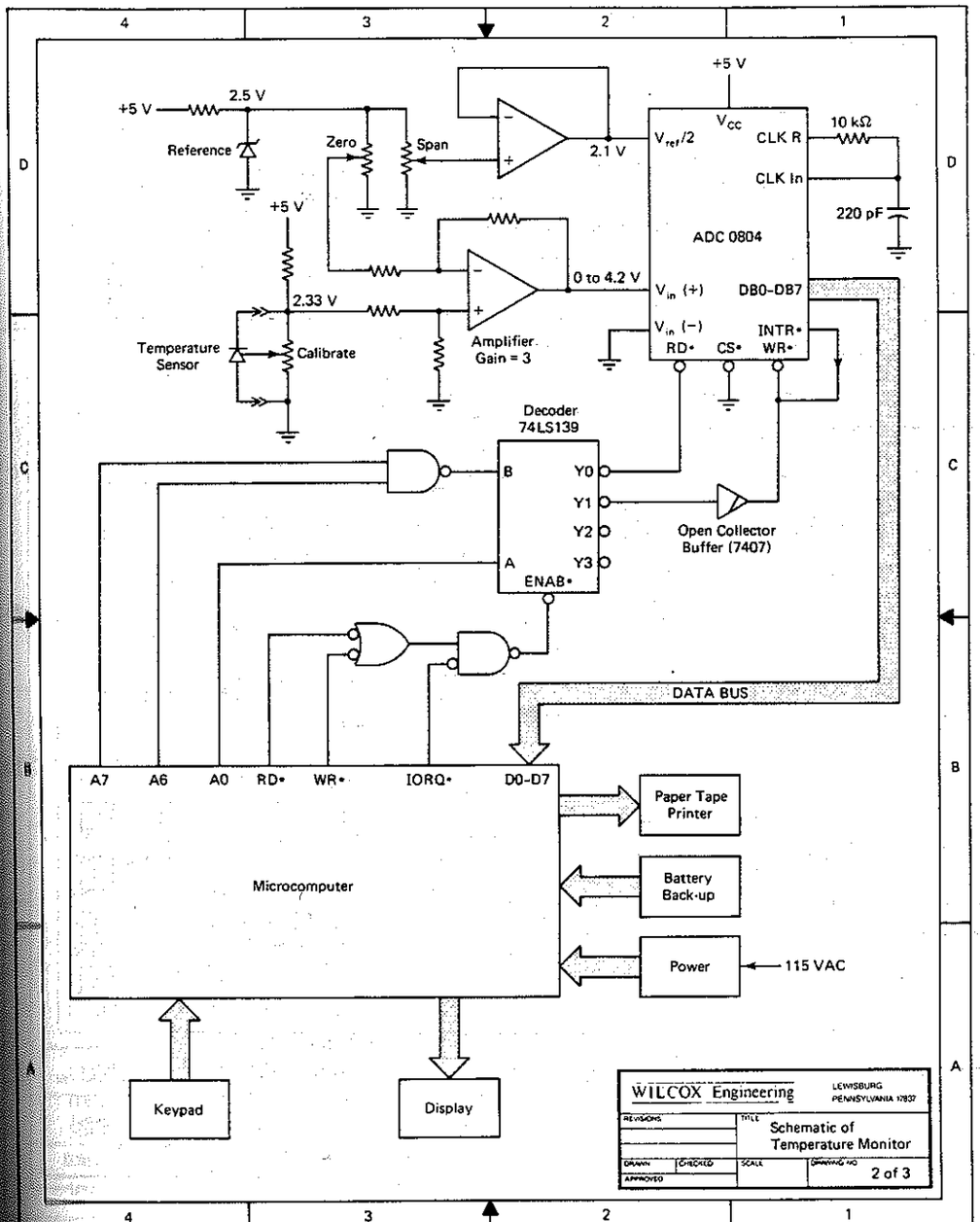
Temperature Monitor
1 of 3



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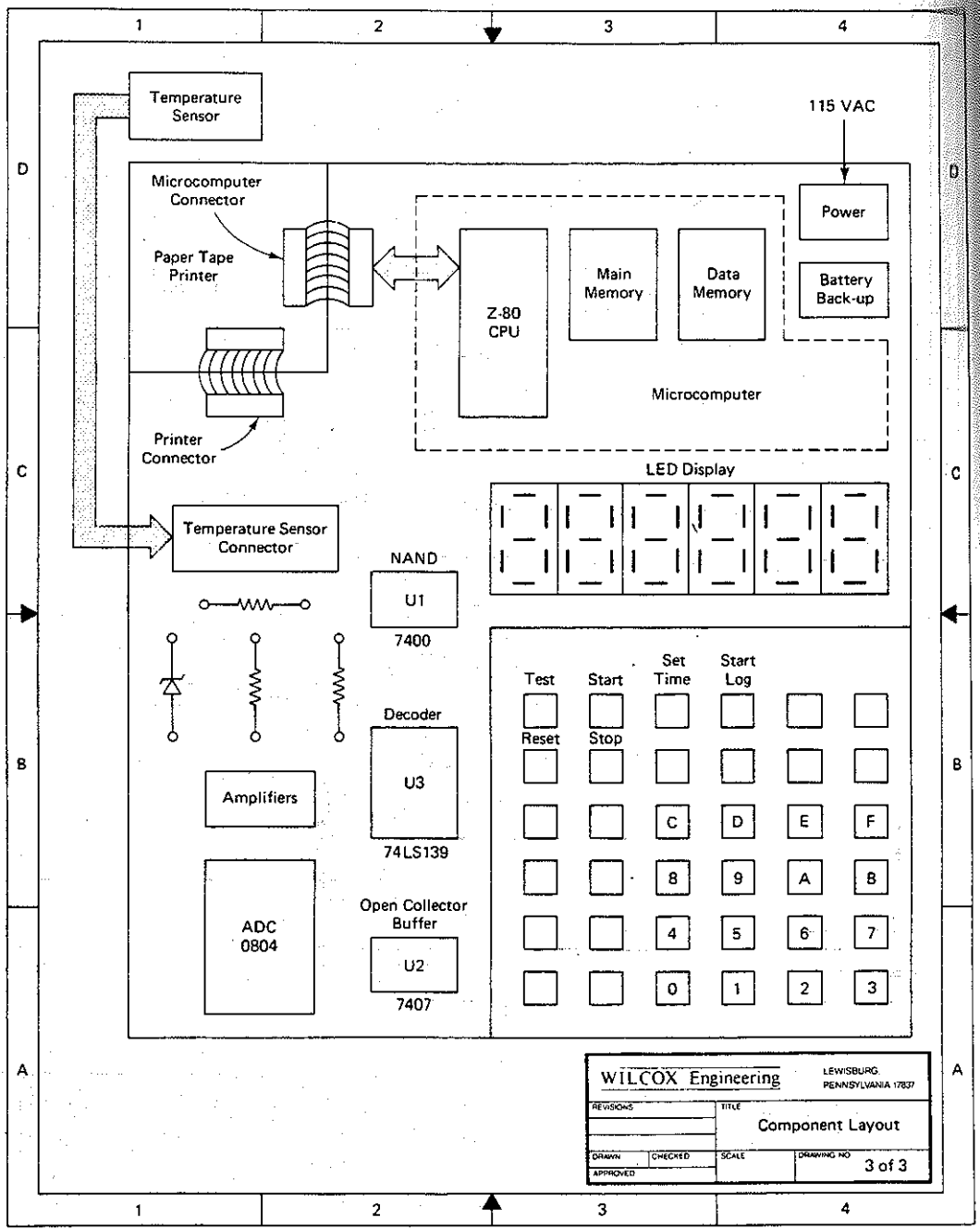
Schematic of Temperature Monitor
2 of 3


1
2
3
4
A
B
C
D
Temperature Sensor
115 VAC
Microcomputer Connector
Paper Tape Printer
Printer Connector
Power
Battery Back-up
Main Memory
Data Memory
Z-80 CPU
Microcomputer
LED Display
Temperature Sensor Connector
NAND
U1
7400
Decoder
U3
74LS139
Amplifiers
ADC 0804
Open Collector Buffer
U2
7407
Test
Start
Set Time
Start Log
Reset
Stop
C
D
E
F
8
9
A
B
4
5
6
7
0
1
2
3
WILCOX Engineering
LEWISBURG PENNSYLVANIA 17837
REVISIONS
TITLE
Component Layout
DRAWN
CHECKED
APPROVED
SCALE
DRAWING NO
3 of 3

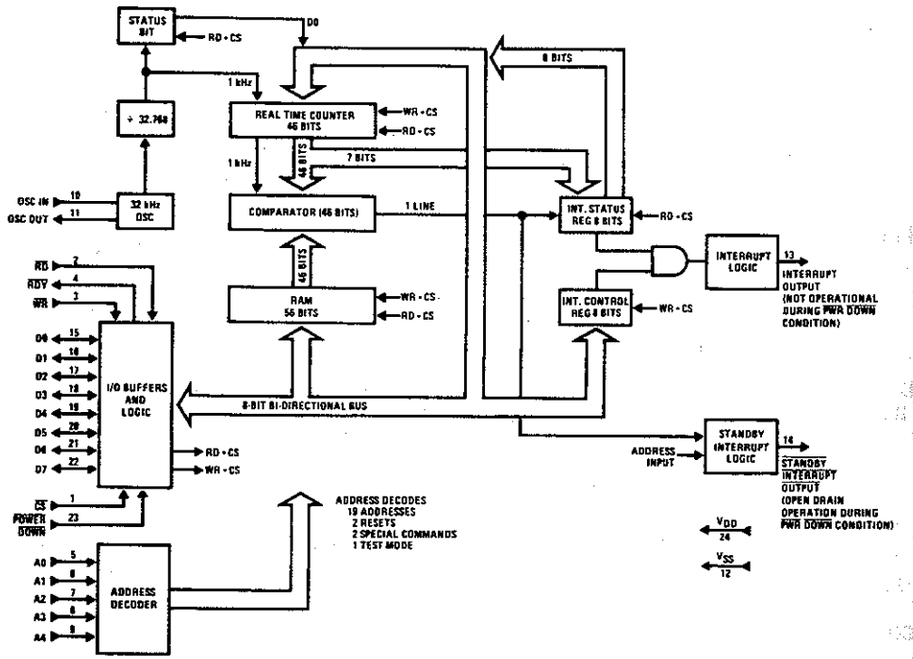


Figure 5.6 Block diagram of the MM58167A real-time clock. (Courtesy National Semiconductor Corp.)

normally completes within 500 ns. However, for I/O devices that require substantial access times, the bus cycle can be extended by adding a number of wait states, as in Figure 5.8. To find out if wait states are required during any read or write bus cycle, the bus master (the CPU) samples the RDY line at the rising edge of the system clock in Bus State 2 (BS2). If the RDY line is found low, then a wait state (BSw) is inserted immediately after BS2; if the RDY is still low a bus state later, then yet another wait state is inserted. Wait states continue to be added until RDY finally goes high; at that point, the bus cycle concludes with BS3.

The MM58167A clock requires wait states in the bus cycle because of its slow access time. For a clock-read operation, the time required from a valid address until the output data is valid might range from 500 ns to the specified maximum of 1050 ns, far longer than the time required for a normal bus cycle (i.e., 167 ns × 3 = 500 ns). The read cycle of a typical 6-MHz IEEE-696 system is shown in Figure 5.8, with approximate times to scale. Notice that the example timing diagram includes a total of three wait states to make up for the slow access time.

The normal S-100 requirement is that the RDY line be low at the end of BS1 if waits are required in a bus cycle. In the clock case, however, this is impossible: the clock

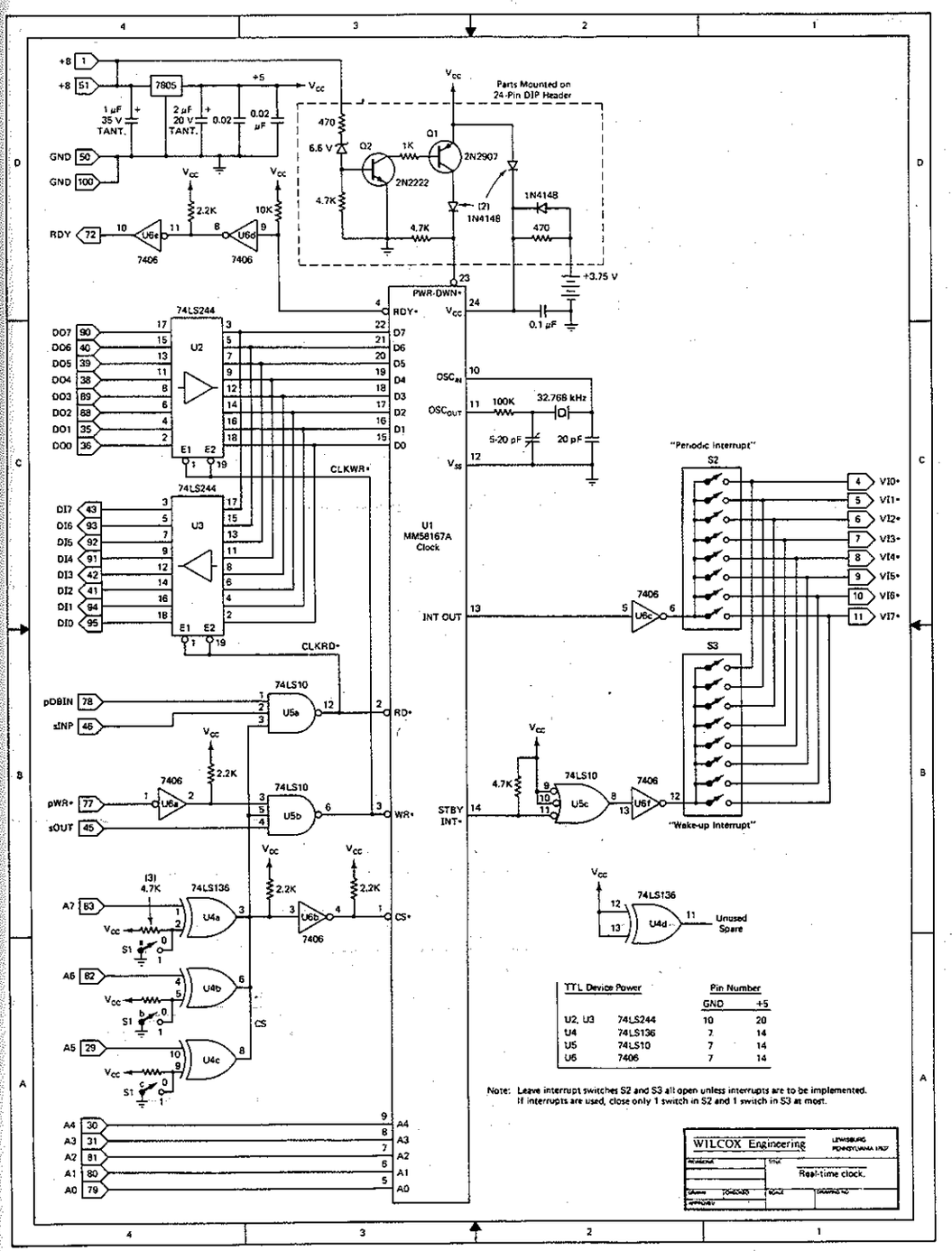


Figure 5.7 Real-time clock schematic drawn on zonal-coordinate paper.