A TASTE OF EAGLE

SDP 2010

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WHY EAGLE?

- Required for Senior Design Project
- Breadboard -> PCB
- Breadboard - prototyping, temporary
  Circuit Board - production, permanent
- Design Requirement?
  - High frequency signals: Clock, Switching Regulators, RF
  - Size, Mechanical Stability, etc.

WHAT IS EAGLE?

- EAGLE **is:**
  - A schematic and layout editor
  - A management tool for CAD drawings
  - A generator of machine files for board manufacture
- EAGLE **is not:**
  - A simulation tool
  - A development environment
  - A Psychic

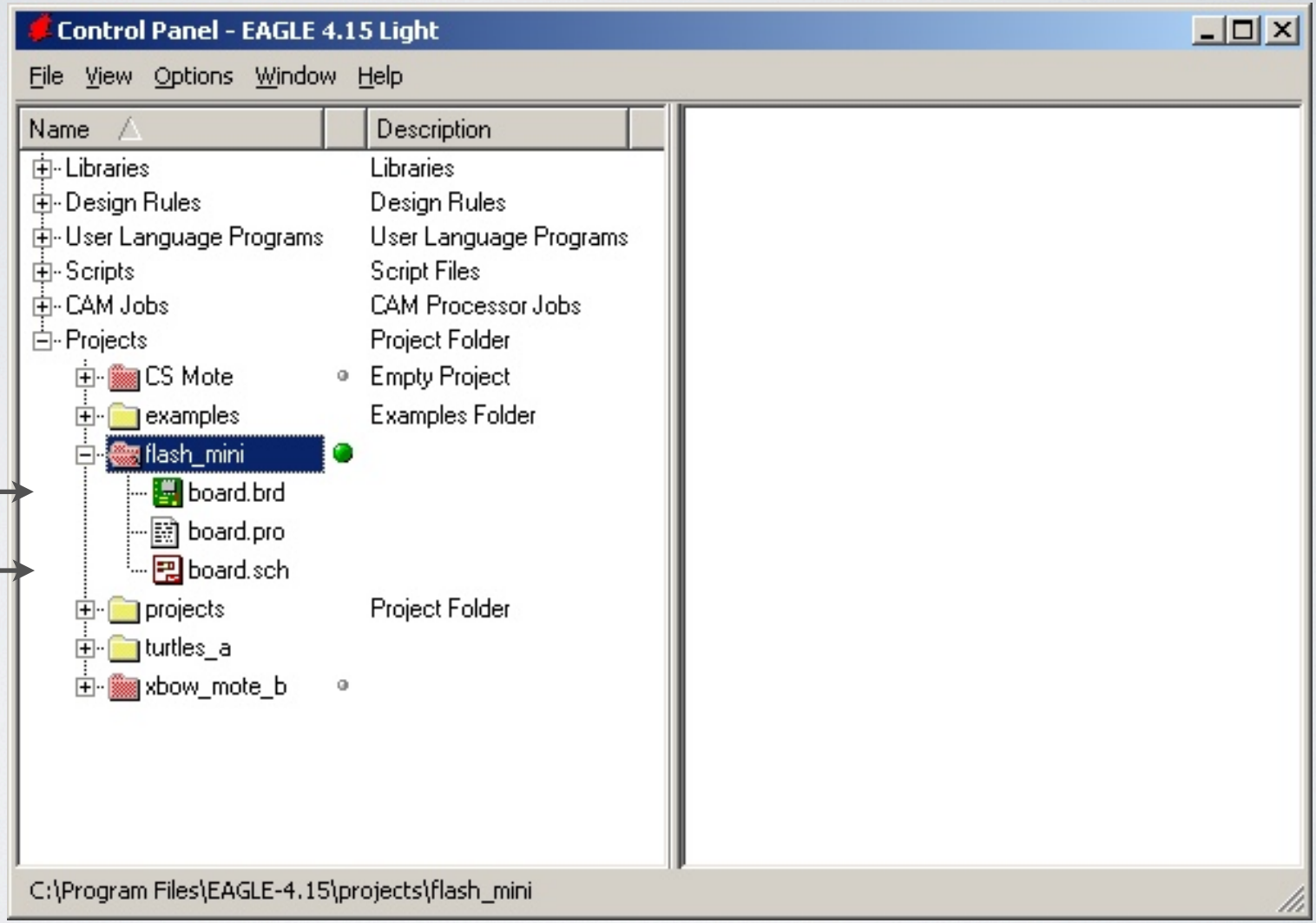
OUTLINE

1. Drawing an Eagle Schematic (a la Orcad)
2. Creating Layout from Schematic (a la Cadence)
3. Manufacturing Rules
4. Generating CAM Files (a la gcc)
5. Creating a new library part
6. Tips

TERMS

- **Footprint**: what a part looks like on the board (Physical connections to pins)
- **Airwire**: a line in the layout indicating a connection that needs to be made
- **Silkscreen**: notation on PCB (no electrical connection)
- **Net**: connections between a group of pins (used to make schematic more readable)

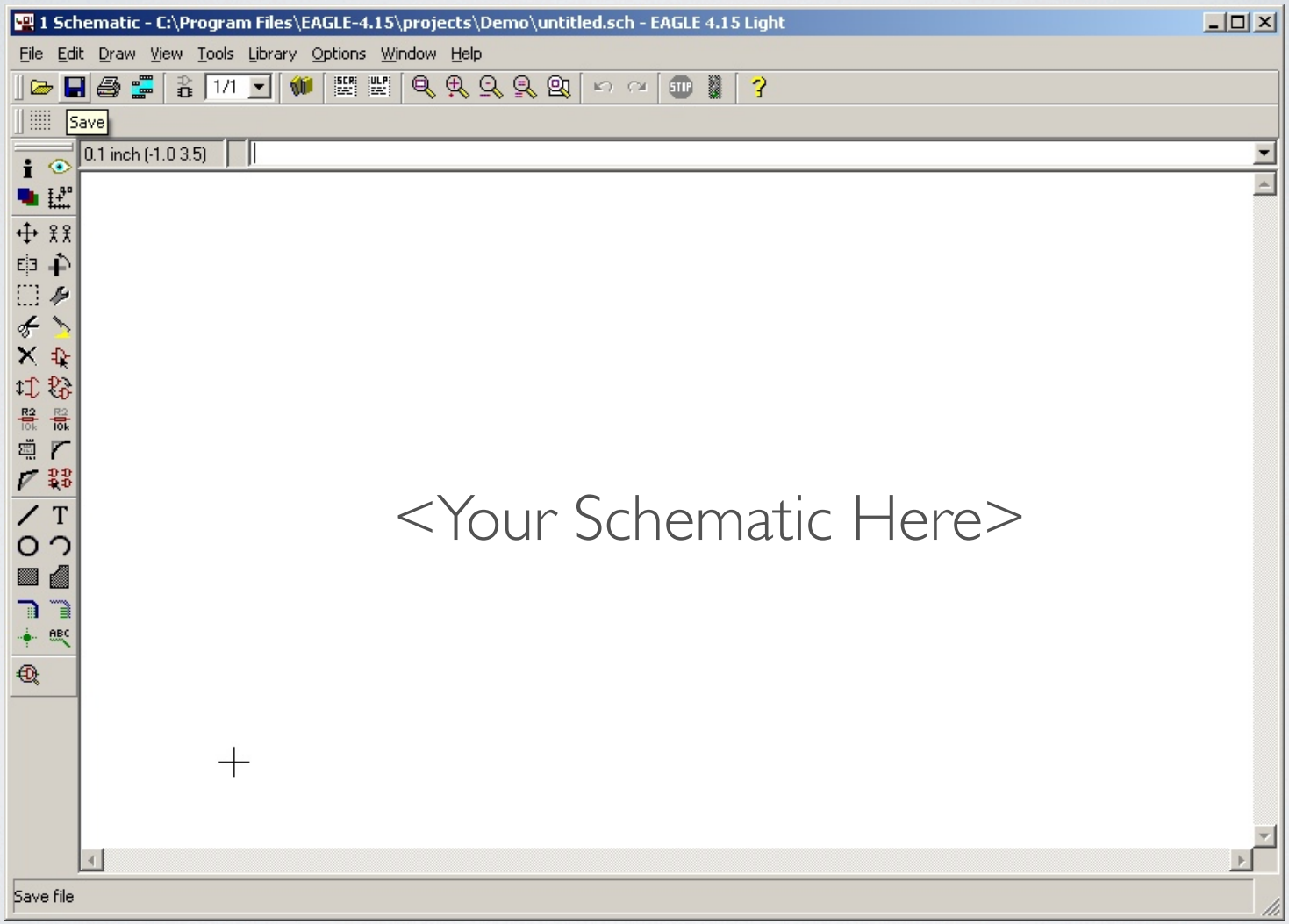
CONTROL PANEL



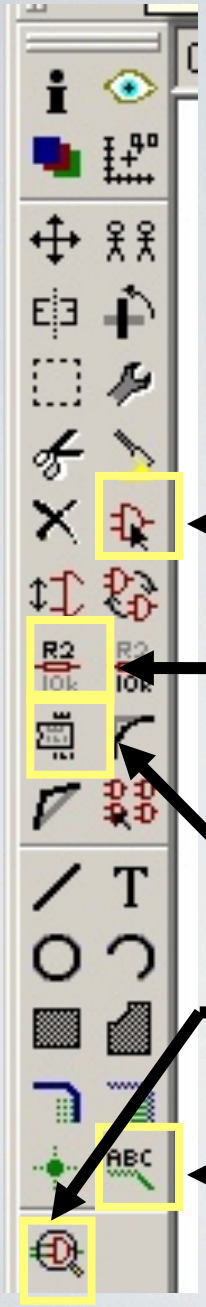
Board →

Schematic →

SCHEMATIC EDITOR



TOOLBAR



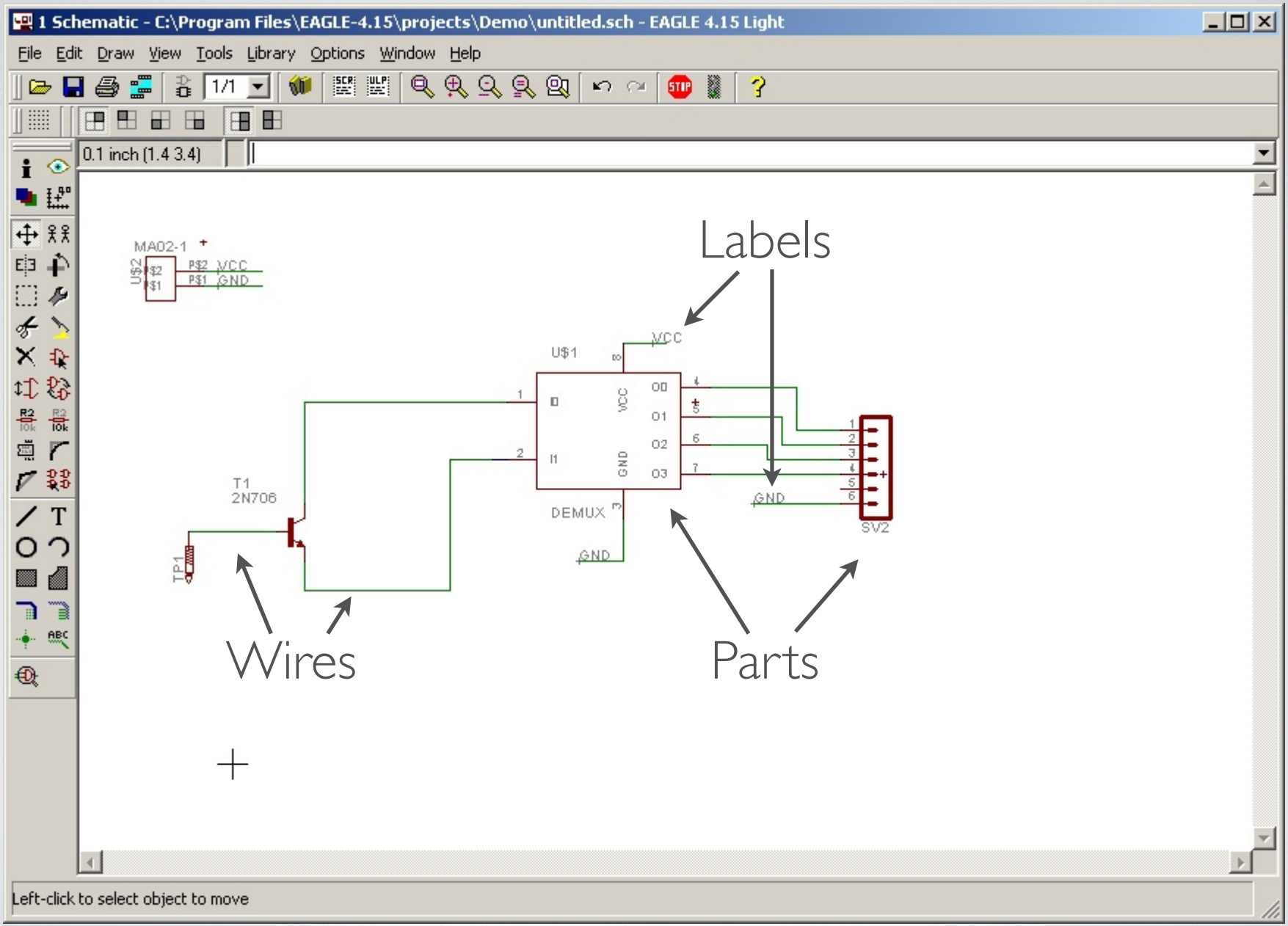
Add Part from library (see control panel)

Name: identify parts and signals

Smash: move pieces of part
e.g. Name, Value

Electrical rule check: Useful to
check for shorts, not much else

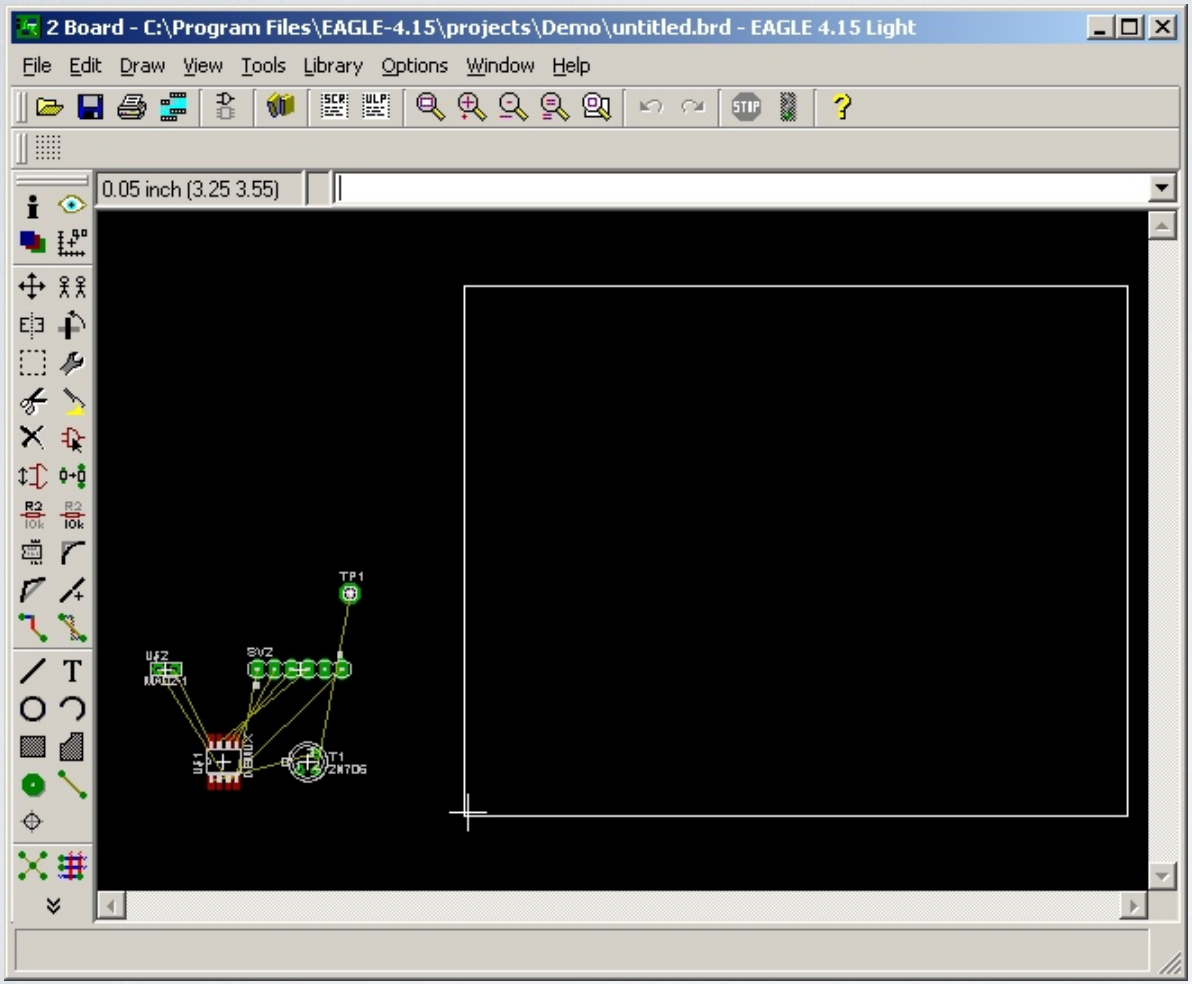
Label: use liberally, can
be difficult to follow wires


1 Schematic - C:\Program Files\EAGLE-4.15\projects\Demo\untitled.sch - EAGLE 4.15 Light
File Edit Draw View Tools Library Options Window Help
0.1 inch (1.4 3.4)
Labels
MA02-1
U$2
P$2 VCC
P$1 GND
U$1
VCC
GND
DEMUX
T1
2N706
TP1
SV2
Wires
Parts
Left-click to select object to move

COMMONLY USED LIBRARIES:

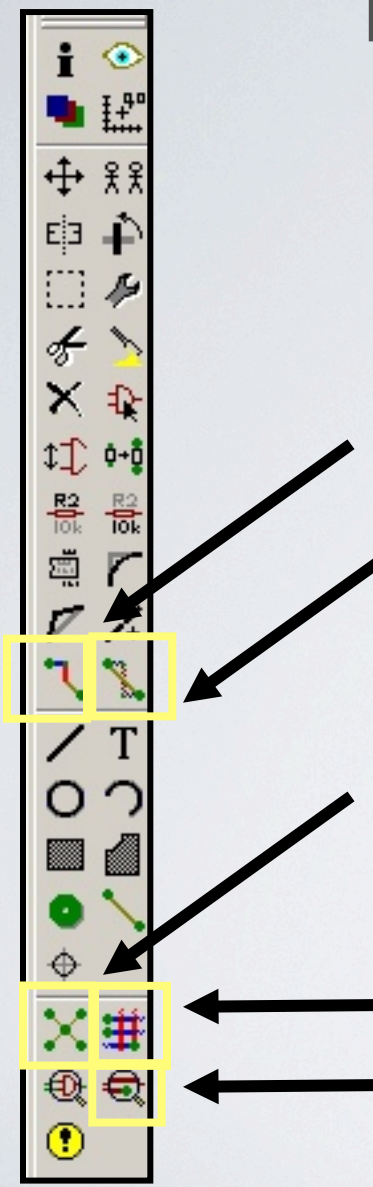
- rcl – resistors, capacitors, inductors
- con-lstb, con-lsta – standard connectors
- con-subd – DB-# connectors
- con-coax – SMA, etc
- linear – op-amps
- solpad – extraneous connections, test pads
- Additional libraries can be found at: http://www.cadsoft.de/download.htm

LAYOUT EDITOR



- Red: top
- Blue: bottom
- Green: through-hole
- White: dimensions & silk screen
- Adjust dimensions with Move

LAYOUT TOOLBAR



Route

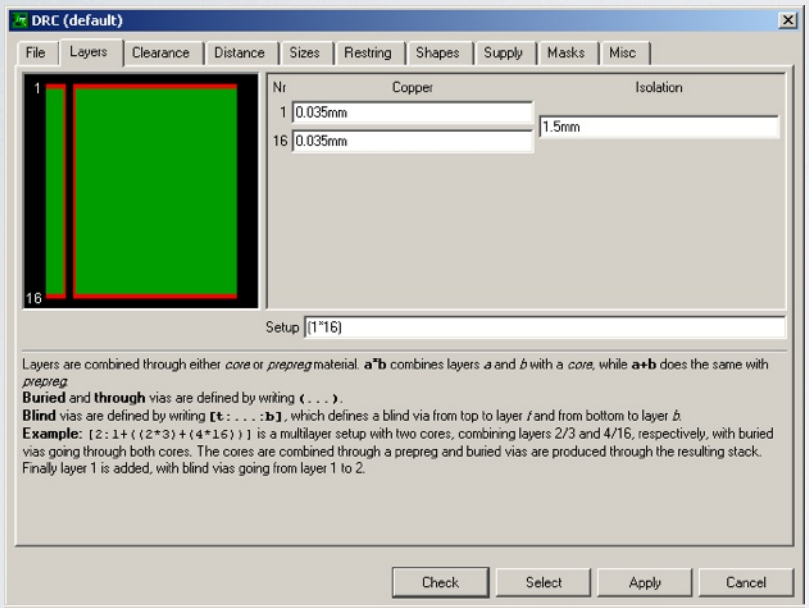
Un-Route

Ratsnest – redraw air wires

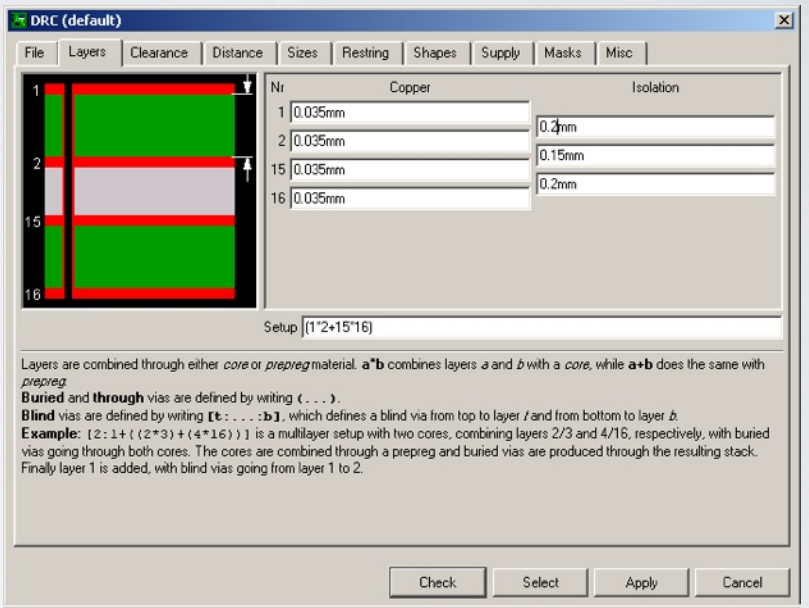
AutoRoute – needs guidance

DRC – Set & Check clearances/layers

DRC - LAYERS

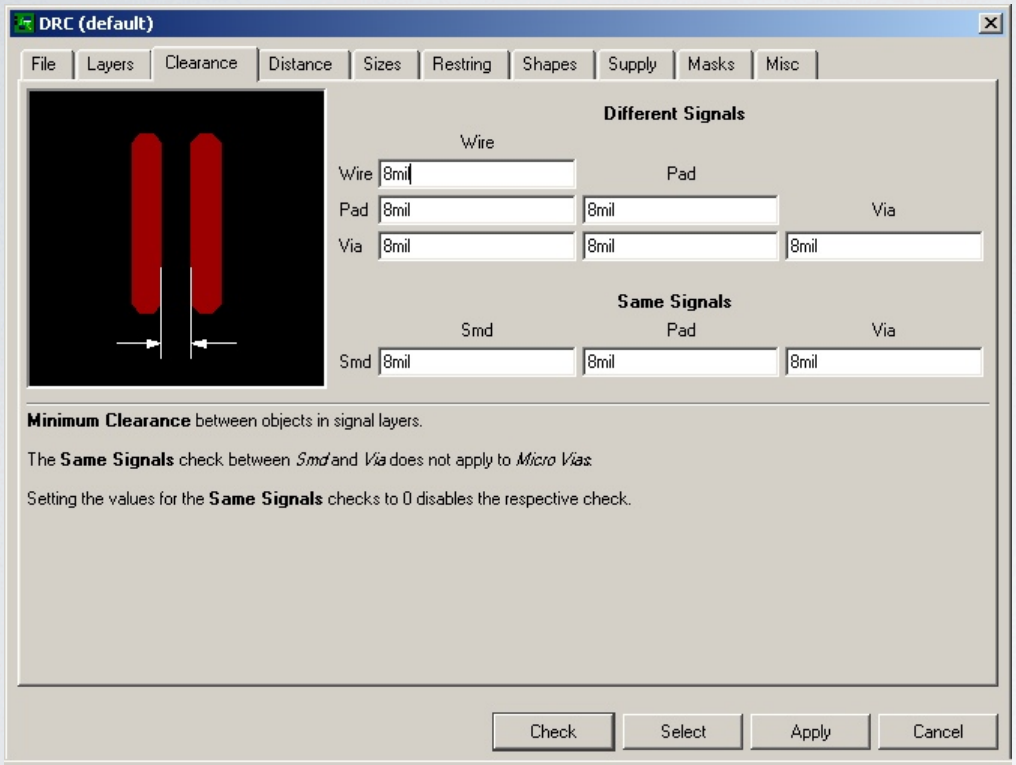


Setup: (1*16)
Two Layers



Setup: (1*2+15*16)
Four Layers
(Not available in Evaluation version)

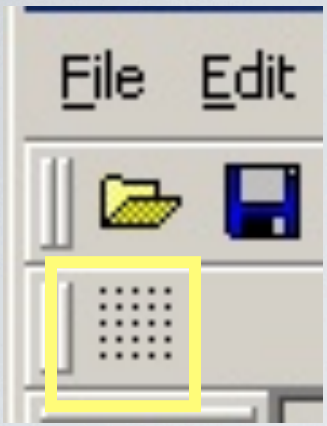
DRC - CLEARANCES



- Specified by board house
- Larger => Cheaper
- 6/6 is small, up to 10/10+
- Careful: some SMT packages require small clearances!

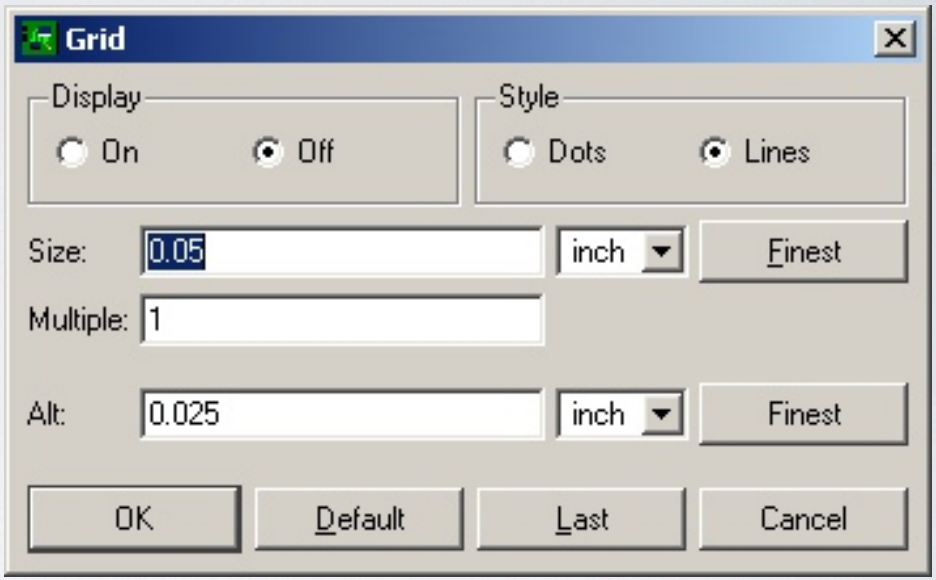
Also check: minimum drill size.
12.5 is safe

GRID (FOR AUTOROUTE)



Normal snap

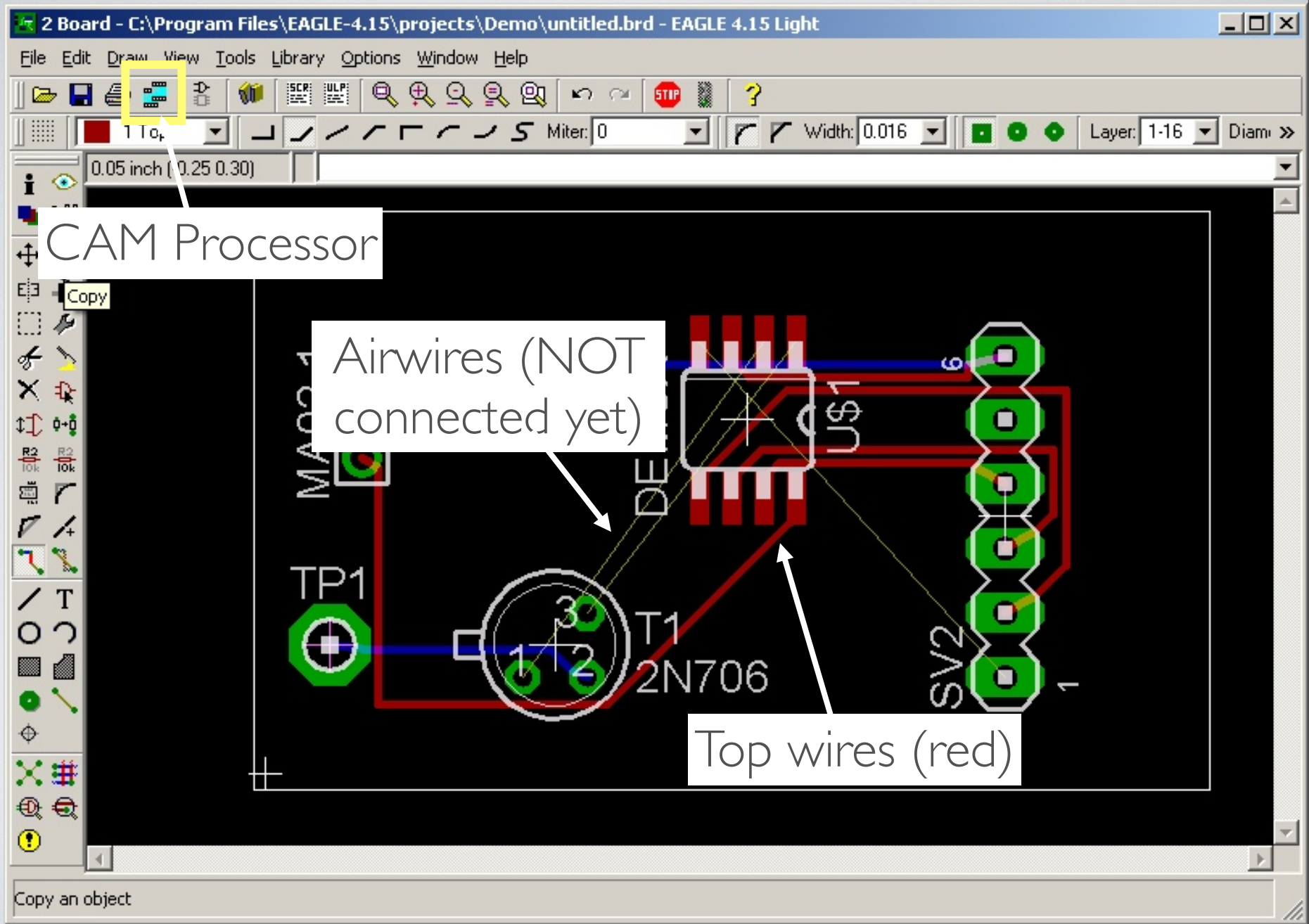
Snap while holding 'alt'



Also set grid in Autoroute options: smaller grid gives router more flexibility, but takes longer to route

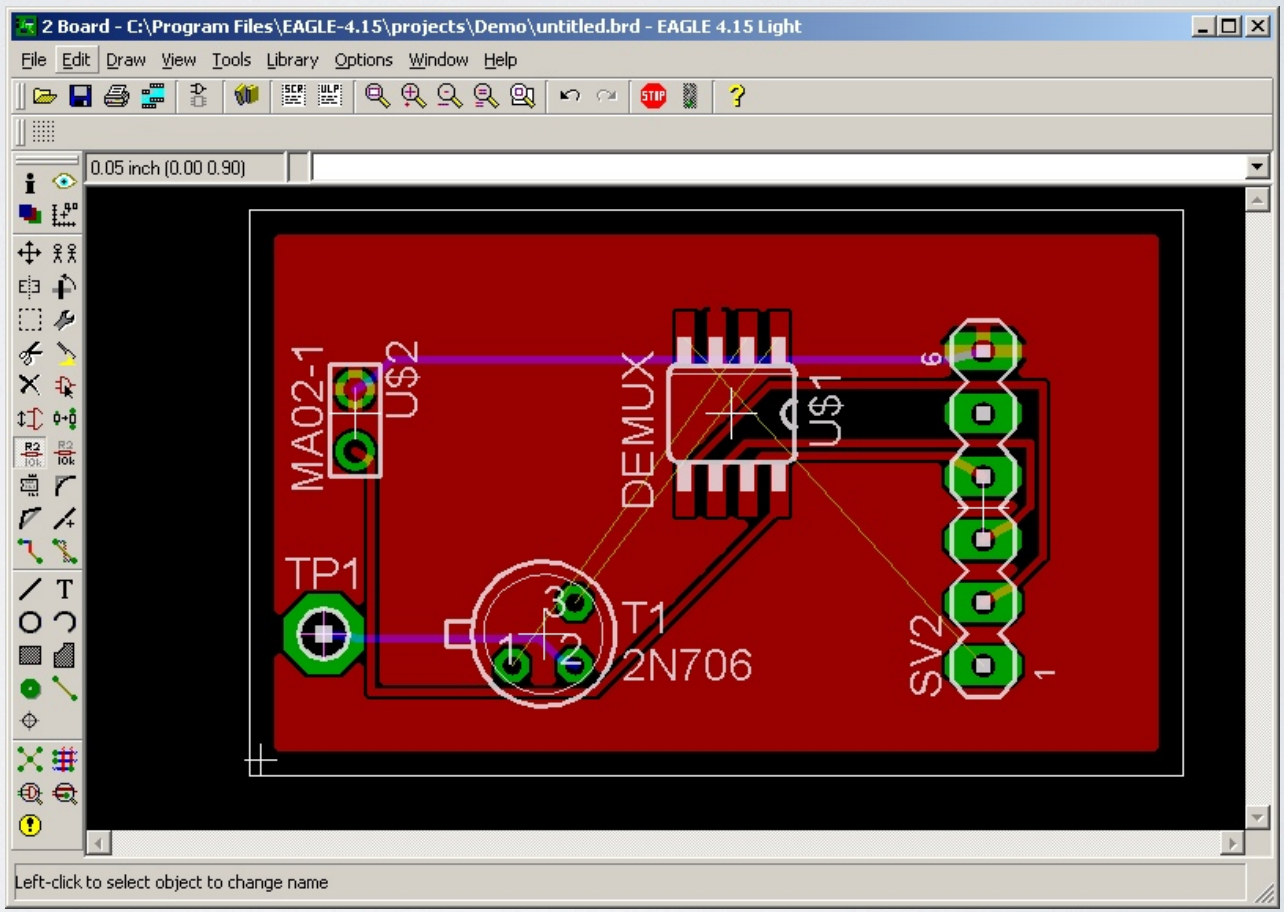
ROUTING

- High-current traces should be WIDE => less resistance => less voltage drop
- Route power & ground first, "by hand" (fat traces)
- Especially if you are using SMD parts, **READ** the layout section of the data sheet
  - Anecdotal: Switching Regulators will self-destruct if their passive components are too far away, or traces are too small
- Avoid right angles
- Keep noisy signals isolated from non-noisy signals
- Use ground planes for sensitive (RF?) designs


2 Board - C:\Program Files\EAGLE-4.15\projects\Demo\untitled.brd - EAGLE 4.15 Light
File Edit Draw View Tools Library Options Window Help
Miter: 0
Width: 0.016
Layer: 1-16
CAM Processor
Copy
Airwires (NOT connected yet)
TP1
T1
2N706
SV2
Top wires (red)
Copy an object

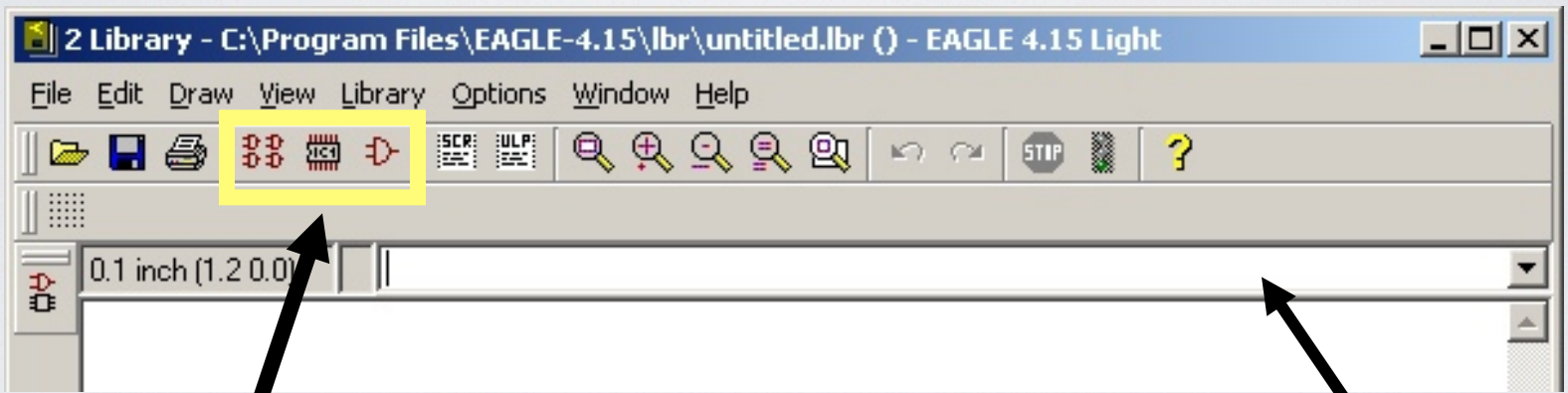
POLYGON TOOL

- For large copper areas. Draw polygon, name (with net name), hit 'ratsnest' to fill



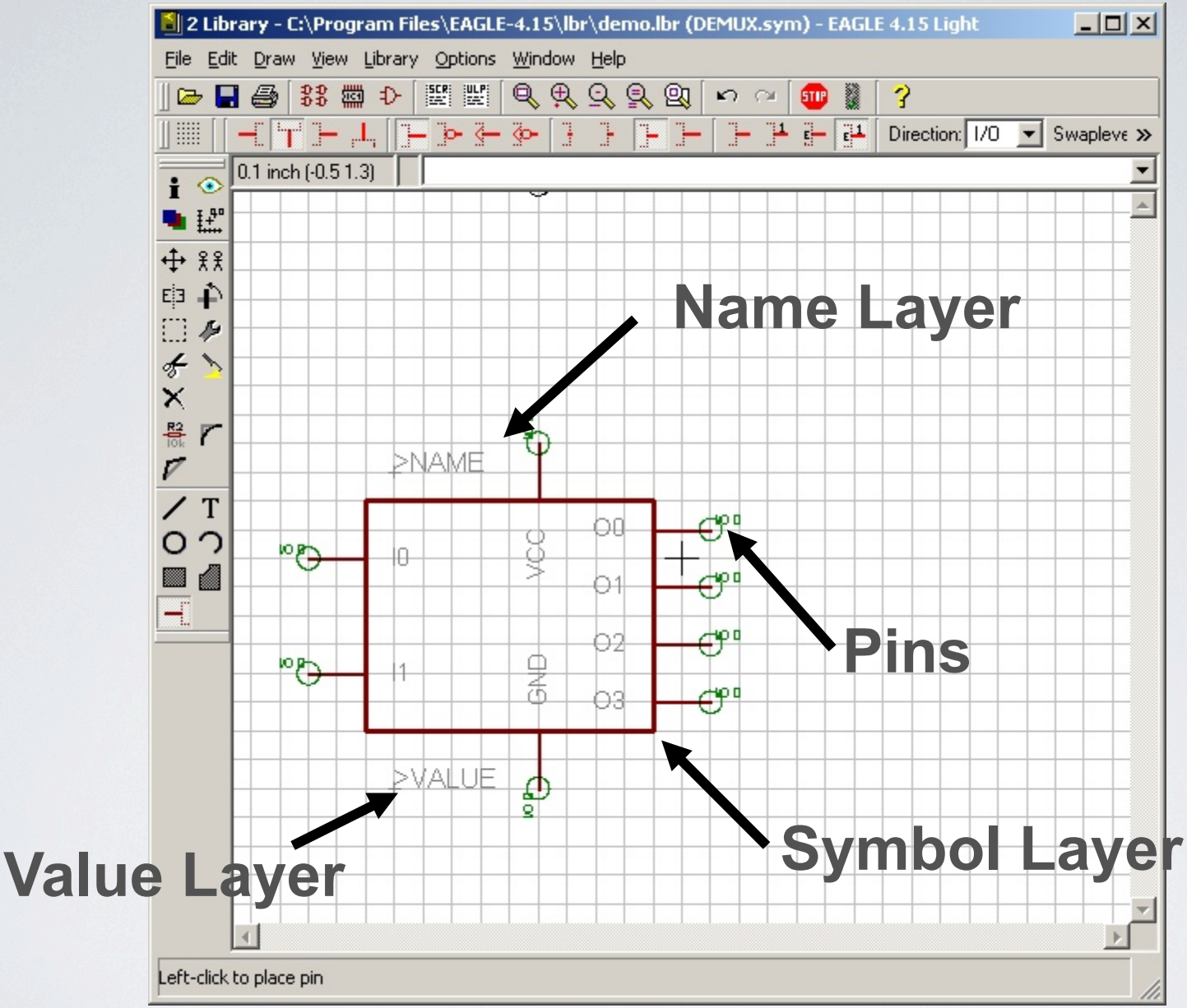
MAKING A PART

- Symbol + Footprint = Device
- Instance of device used in schematic



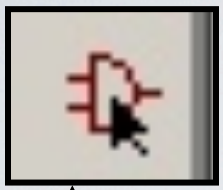
Create/Edit
Device, Footprint, Symbol

Command bar

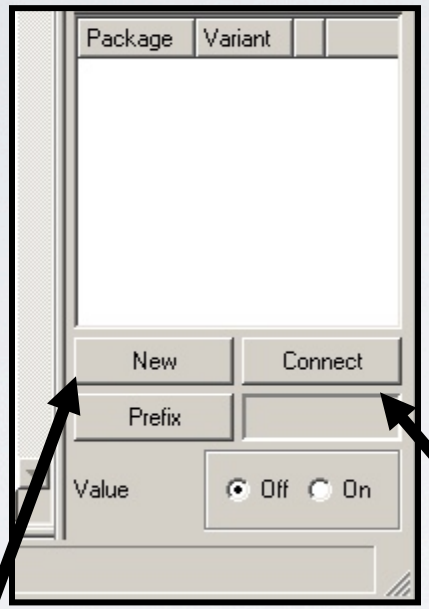


Learning command line can accelerate common tasks (see sparkfun!)

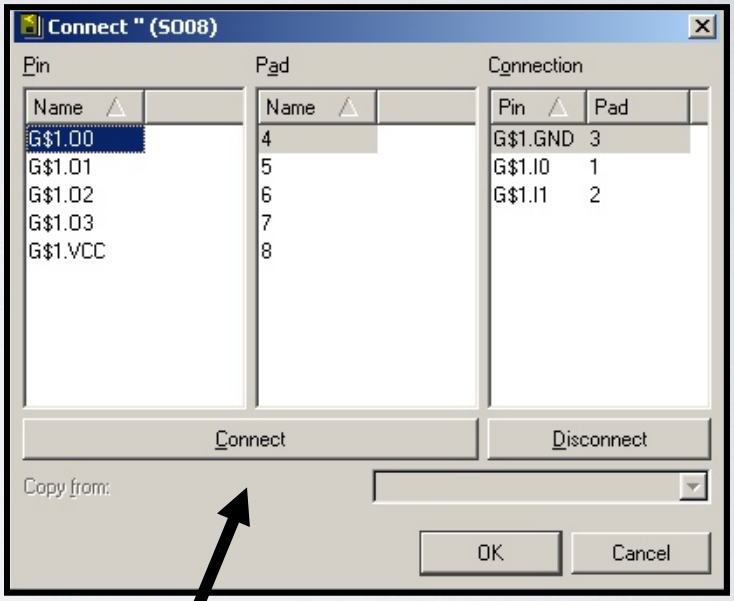
CONNECTING THE DEVICE:



Add symbol to device



Make new package, Choose footprint



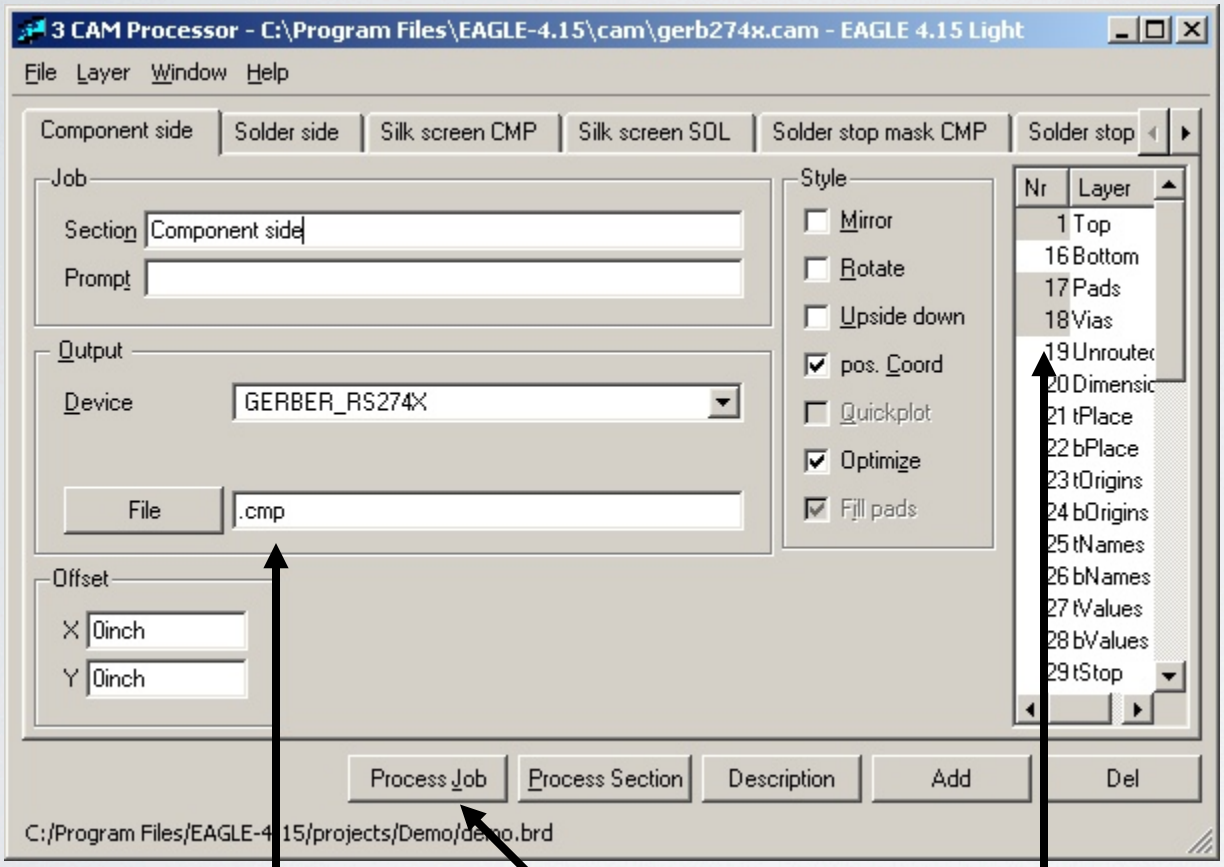
Connect symbol pins to footprint pads

Save library, and "use" it through control panel

IF YOU NEED TO MAKE YOUR OWN FOOTPRINT:

- Datasheet will have section giving mechanical requirements of part
- Remember to mark pin 1 on something that will be printed
- Put >NAME and >VALUE on the respective layers
- Print the footprint in actual size; check to ensure the part will fit on the pads. It's very easy to make mistakes with units.

CAM PROCESSING: FILES FOR BOARD HOUSE



File Extension

Generates CAM data

Selected Layers

CAM PROCESSING

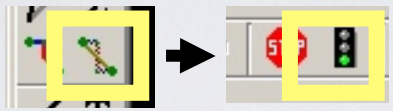
- Two jobs. Use File->open:
  - gerb274x (copper + silkscreen data)
  - excellon (drill data)
- Add (a) section(s) if doing silkscreen on both sides, or additional layers
- Cheap boards have no silkscreen (good luck assembling!)
  - put text on the Top or Bottom copper layers
  - make sure there are no accidental connections
- Double check output machine files with Agnostic Gerber Viewer
  - Free viewer available at: http://www.pentalogix.com

BOARDHOUSES

- Advanced Circuits: http://www.4pcb.com
  - Automated, Free design rule check, results e-mailed within an hour.
  - $33 per 2-layer board
  - Free Food
- PCB Fab Express: http://www.pcbfabexpress.com
  - Cheapest prices – A few dollars per board
  - Cheap boards are minimal – no solder mask, silkscreen. May be sufficient for a very simple design.
- Many others…although I have no experience with them.

OTHER NOTES

- ALWAYS run ERC & DRC. Then double-check by eye
- Rip all routing?



- Power/GND planes (multiple layers):
  - in layout, go to 'layer setup' and name a layer $GND or $VCC, or $netname
- Symbol: Multiple pins with same name?
  - VCC$1, VCC$2, VCC$3: anything after $ won't show in schematic
- Net classes: can define different min sizes for different types of connections (pwr vs data)
- Most commands are available from command bar
- Minimize vias in design
  - less resistance, sometimes cheaper boards
- Check status bar for: "Autorouter: 100% finished."
  - Otherwise, find what it missed

MORE NOTES

- Have your teammates check your design three times
- Be very careful of tricky, silly mistakes – especially if you designed your own part.
  - ERC and DRC could look fine, but connections may be mirrored
- Don't use BGAs and avoid leadless (pins) packages
  - Difficult to solder, maybe impossible to verify (need test pads)
  - Important, non-trivial signal? Stick it on a test-pad
- Assembly Tip:
  - Test as you go. If VCC and GND short, good luck…

QUESTIONS?