

SDP 2010

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WHY EAGLE?

- Required for Senior Design Project
- Breadboard -> PCB
- Breadboard prototyping, temporary Circuit Board - production, permanent
- Design Requirement?
 - High frequency signals: Clock, Switching Regulators, RF
 - Size, Mechanical Stability, etc.

WHAT IS EAGLE?

• EAGLE is:

- A schematic and layout editor
- A management tool for CAD drawings
- A generator of machine files for board manufacture
- EAGLE is not:
 - A simulation tool
 - A development environment
 - A Psychic

OUTLINE

- 1. Drawing an Eagle Schematic (a la Orcad)
- 2. Creating Layout from Schematic (a la Cadence)
- 3. Manufacturing Rules
- 4. Generating CAM Files (a la gcc)
- 5. Creating a new library part

6. Tips

TERMS

- **Footprint**: what a part looks like on the board (Physical connections to pins)
- **Airwire**: a line in the layout indicating a connection that needs to be made
- **<u>Silkscreen</u>**: notation on PCB (no electrical connection)
- **Net**: connections between a group of pins (used to make schematic more readable)

CONTROL PANEL

	Control Panel - EAGLE 4.1	5 Light	
	<u>File View Options Window</u>	Help	
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	C:\Program Files\EAGLE-4.15\pr	ojects\flash_mini	//

SCHEMATIC EDITOR

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COMMONLY USED LIBRARIES:

- rcl resistors, capacitors, inductors
- con-lstb, con-lsta standard connectors
- con-subd DB-# connectors
- con-coax SMA, etc
- linear op-amps
- solpad extraneous connections, test pads
- Additional libraries can be found at: <u>http://www.cadsoft.de/download.htm</u>

LAYOUT EDITOR



- Red: top
- Blue: bottom
- Green: throughhole
- White: dimensions & silk screen
- Adjust dimensions with Move



DRC - LAYERS

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File Layers Clearance Distance Sizes Restring Shapes Supply Masks Misc	File Layers Clearance Distance Sizes Restring Shapes Supply Masks Misc
Nr Copper Isolation 1 [0.035mm [1.5mm 16 [0.035mm Setup [1*16)	Nr Copper Isolation 1 0.035mm 0.2mm 2 0.035mm 0.15mm 15 0.035mm 0.2mm 16 0.035mm 0.2mm Setup [(1*2+15*16)
Expersion Prepring Buried and through visas are defined by writing (). Bind vias are defined by writing [t:): Bind vias are defined by writing [t:): Bind vias from top to layer / and from bottom to layer /. Example: [2:1+((2*3)+(4*15))]): Bind vias are produced through both cores. The cores are combined through a prepreg and buried vias are produced through the resulting stack. Finally layer 1 is added, with blind vias going from layer 1 to 2. Check Select Apply Cancel	Buried and through visa are defined by writing (). Blind visa are defined by writing (t:). Example: (t:L) + (t:2*3) + (t*16) it is a writing the cores. combining layers 2/3 and 4/16, respectively, with buriet visa going through both cores. The cores are combined through a prepreg and buried visa are produced through the resulting stack. Finally layer 1 is added, with blind visa going from layer 1 to 2. Check Select Apply Cancel

Setup: (1*16) Two Layers

Setup: (1*2+15*16) Four Layers (Not available in Evaluation version)

DRC - CLEARANCES

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Also check: minimum drill size. 12.5 is safe Specified by board house

- Larger => Cheaper
- 6/6 is small, up to 10/10+
- Careful: some SMT packages require small clearances!

Eile Edit GRID (FC	DR AUTOROUTE
	Display Style C On Off Off Dots O Lines
Normal snap	Size: 0.05 inch 💌 <u>F</u> inest
Snap while	Alt: 0.025 inch ▼ Finest OK Default Last Cancel

Also set grid in Autoroute options: smaller grid gives router more flexibility, but takes longer to route

ROUTING

- High-current traces should be WIDE => less resistance => less voltage drop
- Route power & ground first, "by hand" (fat traces)
- Especially if you are using SMD parts, **READ** the layout section of the data sheet
 - Anecdotal: Switching Regulators will self-destruct if their passive components are too far away, or traces are too small
- Avoid right angles
- Keep noisy signals isolated from non-noisy signals
- Use ground planes for sensitive (RF?) designs



POLYGONTOOL

• For large copper areas. Draw polygon, name (with net name), hit 'ratsnest' to fill



MAKING A PART

- Symbol + Footprint = Device
- Instance of device used in schematic

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Learning command line can accelerate common tasks (see sparkfun!)

CONNECTING THE DEVICE:

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Choose footp	print	to footpri	nt pads	
Save	library, and ''use'' it	through contr	ol panel	
	21			

IF YOU NEED TO MAKE YOUR OWN FOOTPRINT:

- Datasheet will have section giving mechanical requirements of part
- Remember to mark pin I on something that will be printed
- Put >NAME and >VALUE on the respective layers
- Print the footprint in actual size; check to ensure the part will fit on the pads. It's very easy to make mistakes with units.

CAM PROCESSING: FILES FOR BOARD HOUSE

🚰 3 CAM Processor - C:\Program Files\EAGLE-4.15\cam\gerb2	274x.cam - EAGLE 4.15 Lig	ht _ 🗆 🗙
<u>File Layer Window H</u> elp		
Component side Solder side Silk screen CMP Silk screen SO	L Solder stop mask CMP	Solder stop
Job Section Component side Prompt Dutput Device GERBER_RS274X	Style Mirror Botate Upside down ✓ pos. <u>C</u> oord ✓ <u>Quickplot</u> ✓ Optimize ✓ Fjll pads	Nr Layer 1 Top 16 Bottom 17 Pads 18 Vias 19 Unrouted 20 Dimensid 21 tPlace 23 tOrigins 24 bOrigins 25 tNames 26 bNames 27 tValues 28 bValues 29 tStop
Process Job Process Section C:/Program Files/EAGLE-4 15/projects/Demo/depo.brd	Description Add	Del
File Extension Generates C.	AM data Se	elected La

CAM PROCESSING

- Two jobs. Use File->open:
 - gerb274x (copper + silkscreen data)
 - excellon (drill data)
- Add (a) section(s) if doing silkscreen on both sides, or additional layers
- Cheap boards have no silkscreen (good luck assembling!)
 - put text on the Top or Bottom copper layers
 - make sure there are no accidental connections
- Double check output machine files with Agnostic Gerber Viewer
 - Free viewer available at: http://www.pentalogix.com

BOARDHOUSES

- Advanced Circuits: http://www.4pcb.com
 - Automated, Free design rule check, results e-mailed within an hour.
 - \$33 per 2-layer board
 - Free Food
- PCB Fab Express: http://www.pcbfabexpress.com
 - Cheapest prices A few dollars per board
 - Cheap boards are minimal no solder mask, silkscreen. May be sufficient for a very simple design.
- Many others...although I have no experience with them.

OTHER NOTES

- ALWAYS run ERC & DRC. Then double-check by eye
- Rip all routing?



- Power/GND planes (multiple layers):
 - in layout, go to 'layer setup' and name a layer \$GND or \$VCC, or \$netname
- Symbol: Multiple pins with same name?
 - VCC\$1,VCC\$2,VCC\$3: anything after \$ won't show in schematic
- Net classes: can define different min sizes for different types of connections (pwr vs data)
- Most commands are available from command bar
- Minimize vias in design
 - less resistance, sometimes cheaper boards
- Check status bar for: "Autorouter: 100% finished."
 - Otherwise, find what it missed

MORE NOTES

- Have your teammates check your design three times
- Be very careful of tricky, silly mistakes especially if you designed your own part.
 - ERC and DRC could look fine, but connections may be mirrored
- Don't use BGAs and avoid leadless (pins) packages
 - Difficult to solder, maybe impossible to verify (need test pads)
 - Important, non-trivial signal? Stick it on a test-pad
- Assembly Tip:
 - Test as you go. If VCC and GND short, good luck...

QUESTIONS?