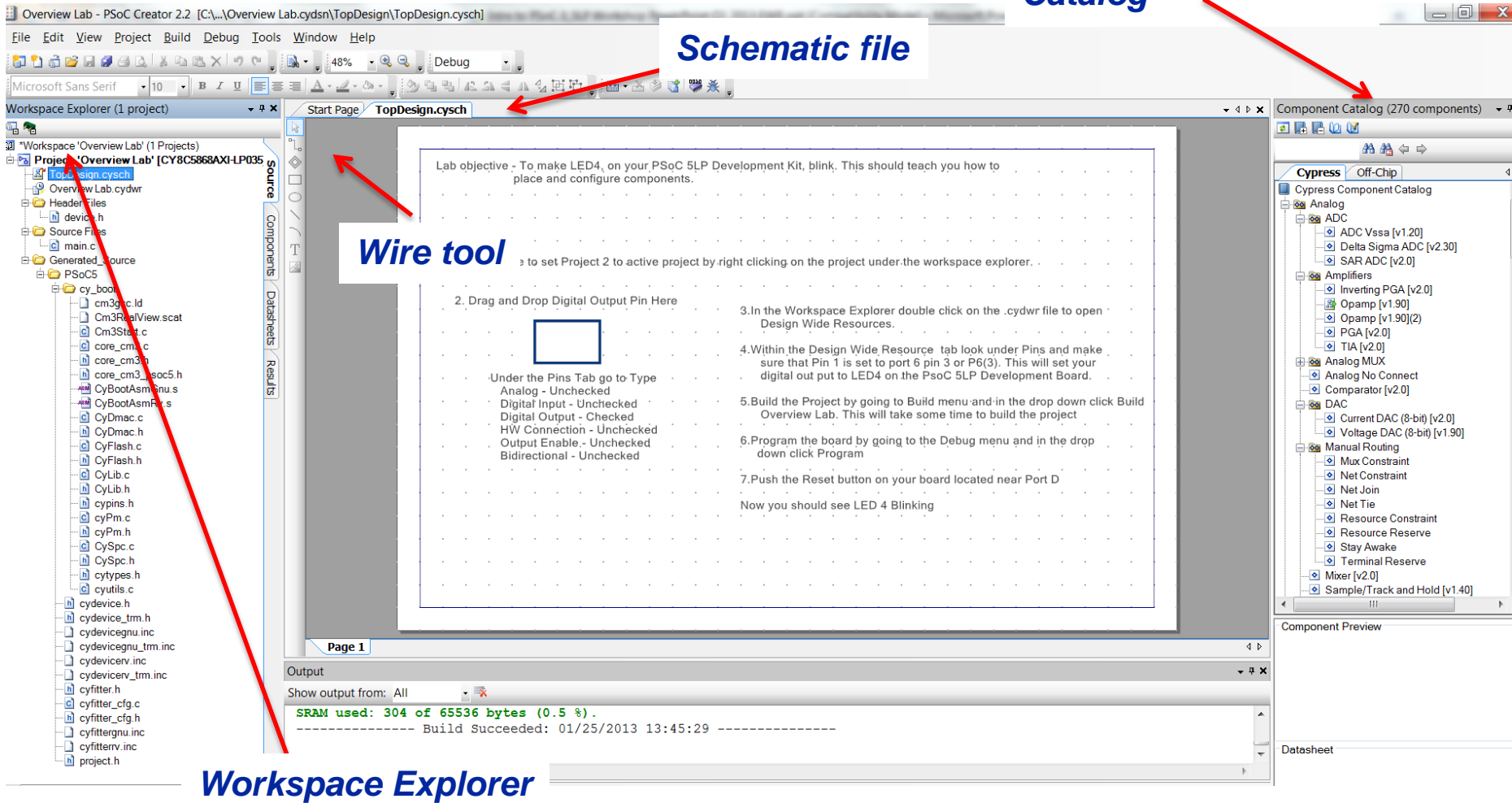

INTRODUCTION TO PSOC 3 AND PSOC 5LP

ARCHITECTURE OVERVIEW

LAB - WALKTHROUGH

PSoC Creator 2.2 Interface

Cypress Component Catalog



The screenshot displays the PSoC Creator 2.2 interface with several key components highlighted by red arrows and labels:

- Workspace Explorer (1 project):** Located on the left, it shows the project structure for "Overview Lab - PSoC Creator 2.2". The "Project" tree is expanded, showing files like "cm3p.c", "cm3p.h", "cm3p.s", "cm3p.t", "cm3p.u", "cm3p.v", "cm3p.w", "cm3p.x", "cm3p.y", "cm3p.z", "cm3p.aa", "cm3p.ab", "cm3p.ac", "cm3p.ad", "cm3p.ae", "cm3p.af", "cm3p.ag", "cm3p.ah", "cm3p.ai", "cm3p.aj", "cm3p.ak", "cm3p.al", "cm3p.am", "cm3p.an", "cm3p.ao", "cm3p.ap", "cm3p.aq", "cm3p.ar", "cm3p.as", "cm3p.at", "cm3p.au", "cm3p.av", "cm3p.aw", "cm3p.ax", "cm3p.ay", "cm3p.az", "cm3p.ba", "cm3p.bb", "cm3p.bc", "cm3p.bd", "cm3p.be", "cm3p bf", "cm3p.bg", "cm3p.bh", "cm3p.bi", "cm3p.bj", "cm3p.bk", "cm3p.bl", "cm3p bm", "cm3p.bn", "cm3p.bo", "cm3p.bp", "cm3p bq", "cm3p.br", "cm3p.bs", "cm3p.bt", "cm3p.bu", "cm3p.bv", "cm3p.bw", "cm3p.bx", "cm3p.by", "cm3p.bz", "cm3p.ca", "cm3p.cb", "cm3p.cc", "cm3p.cd", "cm3p.ce", "cm3p.cf", "cm3p.cg", "cm3p.ch", "cm3p.ci", "cm3p.cj", "cm3p ck", "cm3p.cl", "cm3p.cm", "cm3p.cn", "cm3p.co", "cm3p.cp", "cm3p cq", "cm3p.cr", "cm3p.cs", "cm3p.ct", "cm3p.ct", "cm3p.cv", "cm3p.cw", "cm3p.cx", "cm3p.cy", "cm3p.cz", "cm3p.da", "cm3p.db", "cm3p.dc", "cm3p.dd", "cm3p.de", "cm3p.df", "cm3p.dg", "cm3p.dh", "cm3p.di", "cm3p.dj", "cm3p.dk", "cm3p.dl", "cm3p.dm", "cm3p.dn", "cm3p.do", "cm3p.dp", "cm3p dq", "cm3p.dr", "cm3p.ds", "cm3p.dt", "cm3p.du", "cm3p.dv", "cm3p.dw", "cm3p.dx", "cm3p.dy", "cm3p.dz", "cm3p.ea", "cm3p eb", "cm3p.ec", "cm3p.ed", "cm3p.ee", "cm3p.ef", "cm3p eg", "cm3p.eh", "cm3p.ei", "cm3p.ej", "cm3p.ek", "cm3p.el", "cm3p.em", "cm3p.en", "cm3p eo", "cm3p.ep", "cm3p eq", "cm3p.er", "cm3p.es", "cm3p.et", "cm3p.eu", "cm3p.ev", "cm3p ew", "cm3p.ex", "cm3p.ey", "cm3p.ez", "cm3p.fa", "cm3p.fb", "cm3p.fc", "cm3p.fd", "cm3p.fe", "cm3p.ff", "cm3p fg", "cm3p.fh", "cm3p.fi", "cm3p.fj", "cm3p.fk", "cm3p.fl", "cm3p.fm", "cm3p.fn", "cm3p fo", "cm3p.fp", "cm3p fq", "cm3p.fr", "cm3p.fs", "cm3p.ft", "cm3p.fu", "cm3p.fv", "cm3p.fw", "cm3p.fx", "cm3p.fy", "cm3p.fz", "cm3p.ga", "cm3p.gb", "cm3p.gc", "cm3p.gd", "cm3p.ge", "cm3p.gf", "cm3p.gg", "cm3p gh", "cm3p.gi", "cm3p.gj", "cm3p.gk", "cm3p.gl", "cm3p.gm", "cm3p.gn", "cm3p.go", "cm3p.gp", "cm3p.gq", "cm3p.gr", "cm3p.gs", "cm3p.gt", "cm3p.gu", "cm3p.gv", "cm3p.gw", "cm3p.gx", "cm3p.gy", "cm3p.gz", "cm3p.ha", "cm3p.hb", "cm3p.hc", "cm3p.hd", "cm3p.he", "cm3p.hf", "cm3p.hg", "cm3p.hi", "cm3p.hj", "cm3p.hk", "cm3p.hl", "cm3p.hm", "cm3p.hn", "cm3p ho", "cm3p.hp", "cm3p.hq", "cm3p.hr", "cm3p.hs", "cm3p.ht", "cm3p.hu", "cm3p.hv", "cm3p.hw", "cm3p.hx", "cm3p.hy", "cm3p.hz", "cm3p.ia", "cm3p.ib", "cm3p.ic", "cm3p.id", "cm3p.ie", "cm3p.if", "cm3p.ig", "cm3p.ih", "cm3p.ij", "cm3p.ik", "cm3p.il", "cm3p.im", "cm3p.in", "cm3p.io", "cm3p.ip", "cm3p.iq", "cm3p.ir", "cm3p.is", "cm3p.it", "cm3p.iu", "cm3p.iv", "cm3p.iw", "cm3p.ix", "cm3p.iy", "cm3p.iz", "cm3p.ja", "cm3p.jb", "cm3p.jc", "cm3p.jd", "cm3p.je", "cm3p.jf", "cm3p.jg", "cm3p.jh", "cm3p.ji", "cm3p.jj", "cm3p.jk", "cm3p.jl", "cm3p.jm", "cm3p.jn", "cm3p.jo", "cm3p.jp", "cm3p.jq", "cm3p.jr", "cm3p.js", "cm3p.jt", "cm3p.ju", "cm3p.jv", "cm3p.jw", "cm3p.jx", "cm3p.jy", "cm3p.jz", "cm3p.ka", "cm3p.kb", "cm3p.kc", "cm3p.kd", "cm3p.ke", "cm3p.kf", "cm3p.kg", "cm3p.kh", "cm3p.ki", "cm3p.kj", "cm3p.kk", "cm3p.kl", "cm3p.km", "cm3p.kn", "cm3p.ko", "cm3p.kp", "cm3p.kq", "cm3p.kr", "cm3p.ks", "cm3p.kt", "cm3p.ku", "cm3p.kv", "cm3p.kw", "cm3p.kx", "cm3p.ky", "cm3p.kz", "cm3p.la", "cm3p.lb", "cm3p.lc", "cm3p.ld", "cm3p.le", "cm3p.lf", "cm3p.lg", "cm3p.lh", "cm3p.li", "cm3p.lj", "cm3p.lk", "cm3p.ll", "cm3p.lm", "cm3p.ln", "cm3p.lo", "cm3p.lp", "cm3p.lq", "cm3p.lr", "cm3p.ls", "cm3p.lt", "cm3p.lu", "cm3p.lv", "cm3p.lw", "cm3p.lx", "cm3p.ly", "cm3p.lz", "cm3p.ma", "cm3p.mb", "cm3p.mc", "cm3p.md", "cm3p.me", "cm3p.mf", "cm3p.mg", "cm3p.mh", "cm3p.mi", "cm3p.mj", "cm3p.mk", "cm3p.ml", "cm3p.mm", "cm3p.mn", "cm3p.mo", "cm3p.mp", "cm3p.mq", "cm3p.mr", "cm3p.ms", "cm3p.mt", "cm3p.mu", "cm3p.mv", "cm3p.mw", "cm3p.mx", "cm3p.my", "cm3p.mz", "cm3p.na", "cm3p.nb", "cm3p.nc", "cm3p.nd", "cm3p.ne", "cm3p.nf", "cm3p.ng", "cm3p.nh", "cm3p.ni", "cm3p.nj", "cm3p.nk", "cm3p.nl", "cm3p.nm", "cm3p.nn", "cm3p.no", "cm3p.np", "cm3p.nq", "cm3p.nr", "cm3p.ns", "cm3p.nt", "cm3p.nu", "cm3p.nv", "cm3p.nw", "cm3p.nx", "cm3p.ny", "cm3p.nz", "cm3p.oe", "cm3p.of", "cm3p.og", "cm3p.oh", "cm3p.oi", "cm3p.oj", "cm3p.ok", "cm3p.ol", "cm3p.om", "cm3p.on", "cm3p.oo", "cm3p.op", "cm3p.oq", "cm3p.or", "cm3p.os", "cm3p.ot", "cm3p.ou", "cm3p.ov", "cm3p.ow", "cm3p.ox", "cm3p.oy", "cm3p.oz", "cm3p.pa", "cm3p.pb", "cm3p.pc", "cm3p.pd", "cm3p.pe", "cm3p.pf", "cm3p.pg", "cm3p.ph", "cm3p.pi", "cm3p.pj", "cm3p.pk", "cm3p.pl", "cm3p.pm", "cm3p.pn", "cm3p.po", "cm3p.pp", "cm3p.pq", "cm3p.pr", "cm3p.ps", "cm3p.pt", "cm3p.pu", "cm3p.pv", "cm3p.pw", "cm3p.px", "cm3p.py", "cm3p.pz", "cm3p.qa", "cm3p.qb", "cm3p.qc", "cm3p.qd", "cm3p.qe", "cm3p.qf", "cm3p.qg", "cm3p.qh", "cm3p.qi", "cm3p.qj", "cm3p.qk", "cm3p ql", "cm3p.qm", "cm3p.qn", "cm3p.qo", "cm3p.qp", "cm3p.qq", "cm3p.qr", "cm3p.qs", "cm3p.qt", "cm3p.qu", "cm3p.qv", "cm3p.qw", "cm3p.qx", "cm3p.qy", "cm3p.qz", "cm3p.ra", "cm3p.rb", "cm3p.rc", "cm3p.rd", "cm3p.re", "cm3p.rf", "cm3p.rg", "cm3p.rh", "cm3p.ri", "cm3p.rj", "cm3p.rk", "cm3p.rl", "cm3p.rm", "cm3p.rn", "cm3p.ro", "cm3p.rp", "cm3p.rq", "cm3p.rr", "cm3p.rs", "cm3p.rt", "cm3p.ru", "cm3p.rv", "cm3p.rw", "cm3p.rx", "cm3p.ry", "cm3p.rz", "cm3p.sa", "cm3p.sb", "cm3p.sc", "cm3p.sd", "cm3p.se", "cm3p.sf", "cm3p.sg", "cm3p.sh", "cm3p.si", "cm3p.sj", "cm3p.sk", "cm3p.sl", "cm3p.sm", "cm3p.sn", "cm3p.so", "cm3p.sp", "cm3p.sq", "cm3p.sr", "cm3p.ss", "cm3p.st", "cm3p.su", "cm3p.sv", "cm3p.sw", "cm3p.sx", "cm3p.sy", "cm3p.sz", "cm3p.ta", "cm3p.tb", "cm3p.tc", "cm3p.td", "cm3p.te", "cm3p.tf", "cm3p.tg", "cm3p.th", "cm3p.ti", "cm3p.tj", "cm3p.tk", "cm3p.tl", "cm3p.tm", "cm3p.tn", "cm3p.to", "cm3p.tp", "cm3p.tq", "cm3p.tr", "cm3p.ts", "cm3p.tt", "cm3p.tu", "cm3p.tv", "cm3p.tw", "cm3p.tx", "cm3p.ty", "cm3p.tz", "cm3p.ua", "cm3p.ub", "cm3p.uc", "cm3p.ud", "cm3p.ue", "cm3p.uf", "cm3p.ug", "cm3p.uh", "cm3p.ui", "cm3p.uj", "cm3p.uk", "cm3p.ul", "cm3p.um", "cm3p.un", "cm3p.uo", "cm3p.up", "cm3p.uq", "cm3p.ur", "cm3p.us", "cm3p.ut", "cm3p.uu", "cm3p.uv", "cm3p.uw", "cm3p.ux", "cm3p.uy", "cm3p.uz", "cm3p.va", "cm3p.vb", "cm3p.vc", "cm3p.vd", "cm3p.ve", "cm3p.vf", "cm3p.vg", "cm3p.vh", "cm3p.vi", "cm3p.vj", "cm3p.vk", "cm3p.vl", "cm3p.vm", "cm3p.vn", "cm3p.vo", "cm3p.vp", "cm3p.vq", "cm3p.vr", "cm3p.vs", "cm3p.vt", "cm3p.vu", "cm3p.vv", "cm3p.vw", "cm3p.vx", "cm3p.vy", "cm3p.vz", "cm3p.wa", "cm3p.wb", "cm3p.wc", "cm3p.wd", "cm3p.we", "cm3p.wf", "cm3p.wg", "cm3p.wh", "cm3p.wi", "cm3p.wj", "cm3p.wk", "cm3p.wl", "cm3p.wm", "cm3p.wn", "cm3p.wo", "cm3p.wp", "cm3p.wq", "cm3p.wr", "cm3p.ws", "cm3p.wt", "cm3p.wu", "cm3p.wv", "cm3p.ww", "cm3p.wx", "cm3p.wy", "cm3p.wz", "cm3p.xa", "cm3p.xb", "cm3p.xc", "cm3p.xd", "cm3p.xe", "cm3p.xf", "cm3p.xg", "cm3p.xh", "cm3p.xi", "cm3p.xj", "cm3p.xk", "cm3p.xl", "cm3p.xm", "cm3p.xn", "cm3p.xo", "cm3p.xp", "cm3p.xq", "cm3p.xr", "cm3p.xs", "cm3p.xt", "cm3p.xu", "cm3p.xv", "cm3p.xw", "cm3p.xx", "cm3p.xy", "cm3p.xz", "cm3p.ya", "cm3p.yb", "cm3p.yc", "cm3p.yd", "cm3p.ye", "cm3p.yf", "cm3p.yg", "cm3p.yh", "cm3p.yi", "cm3p.yj", "cm3p.yk", "cm3p.yl", "cm3p.ym", "cm3p.yn", "cm3p.yo", "cm3p.yp", "cm3p.yq", "cm3p.yr", "cm3p.ys", "cm3p.yt", "cm3p.yu", "cm3p.yv", "cm3p.yw", "cm3p.yx", "cm3p.yy", "cm3p.yz", "cm3p.za", "cm3p.zb", "cm3p.zc", "cm3p.zd", "cm3p.ze", "cm3p.zf", "cm3p.zg", "cm3p.zh", "cm3p.zi", "cm3p.zj", "cm3p.zk", "cm3p.zl", "cm3p.zm", "cm3p.zn", "cm3p.zo", "cm3p.zp", "cm3p.zq", "cm3p.zr", "cm3p.zs", "cm3p.zt", "cm3p.zu", "cm3p.zv", "cm3p.zw", "cm3p.zx", "cm3p.zy", "cm3p.zz".
- Schematic file:** The main workspace area displays the "TopDesign.cysch" file. It contains a lab objective: "To make LED4, on your PSoC 5LP Development Kit, blink. This should teach you how to place and configure components." Below this, there are instructions for setting up the project and configuring the digital output pin. A red arrow points to the "Wire tool" icon in the toolbar.
- Wire tool:** A red arrow points to the "Wire tool" icon in the toolbar, which is used for connecting components in the schematic.
- Component Catalog (270 components):** Located on the right, it lists various components available for use in the schematic. The "Cypress" tab is selected, showing a list of components including ADC, Amplifiers, Analog MUX, DAC, Manual Routing, and Mixers.
- Workspace Explorer:** A red arrow points to the "Workspace Explorer" on the left, which shows the project structure and the list of components in the project.

The bottom status bar shows the output of the build process:

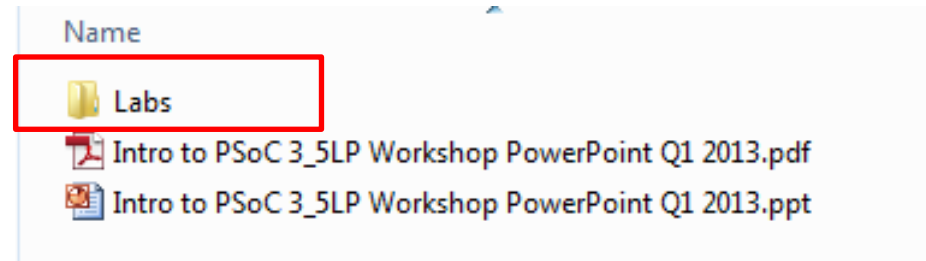
```
Output
Show output from: All
SRAM used: 304 of 65536 bytes (0.5 %).
----- Build Succeeded: 01/25/2013 13:45:29 -----
```

Lab Objective

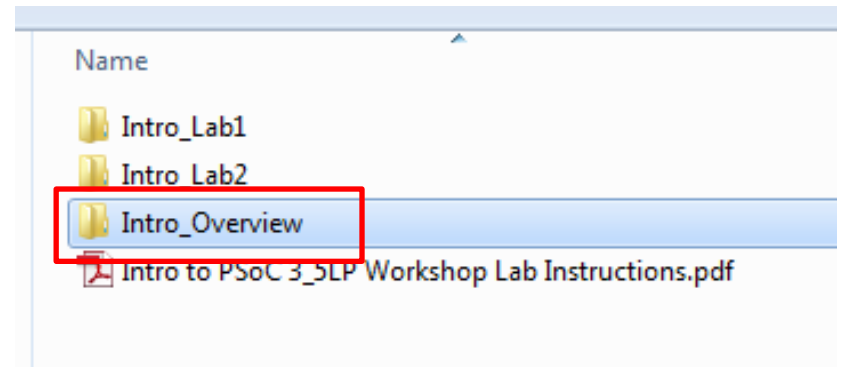
- To make LED4 on your PSoC Development Kit blink.
- To learn how to place and configure components in PSoC Creator

Architecture Overview Lab

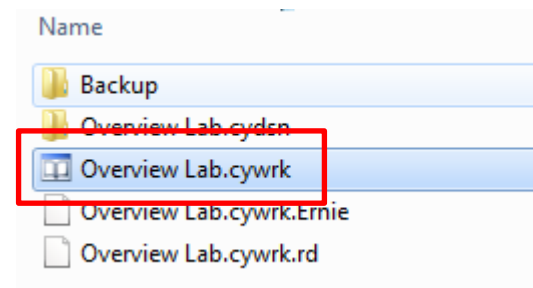
- Open Labs Directory



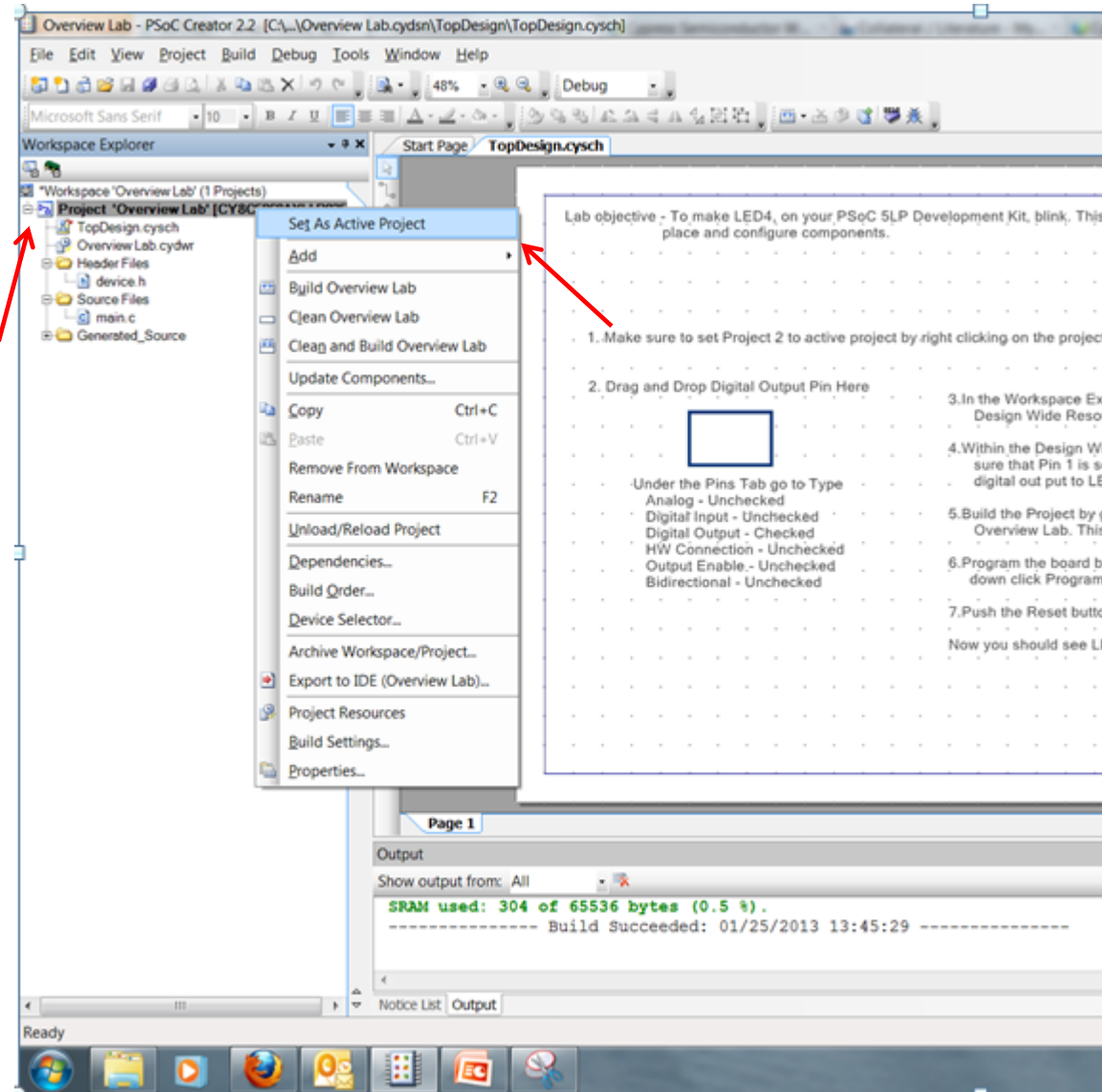
- Open Intro_Overview Directory



- Double Click 'Overview Lab.cywrk'



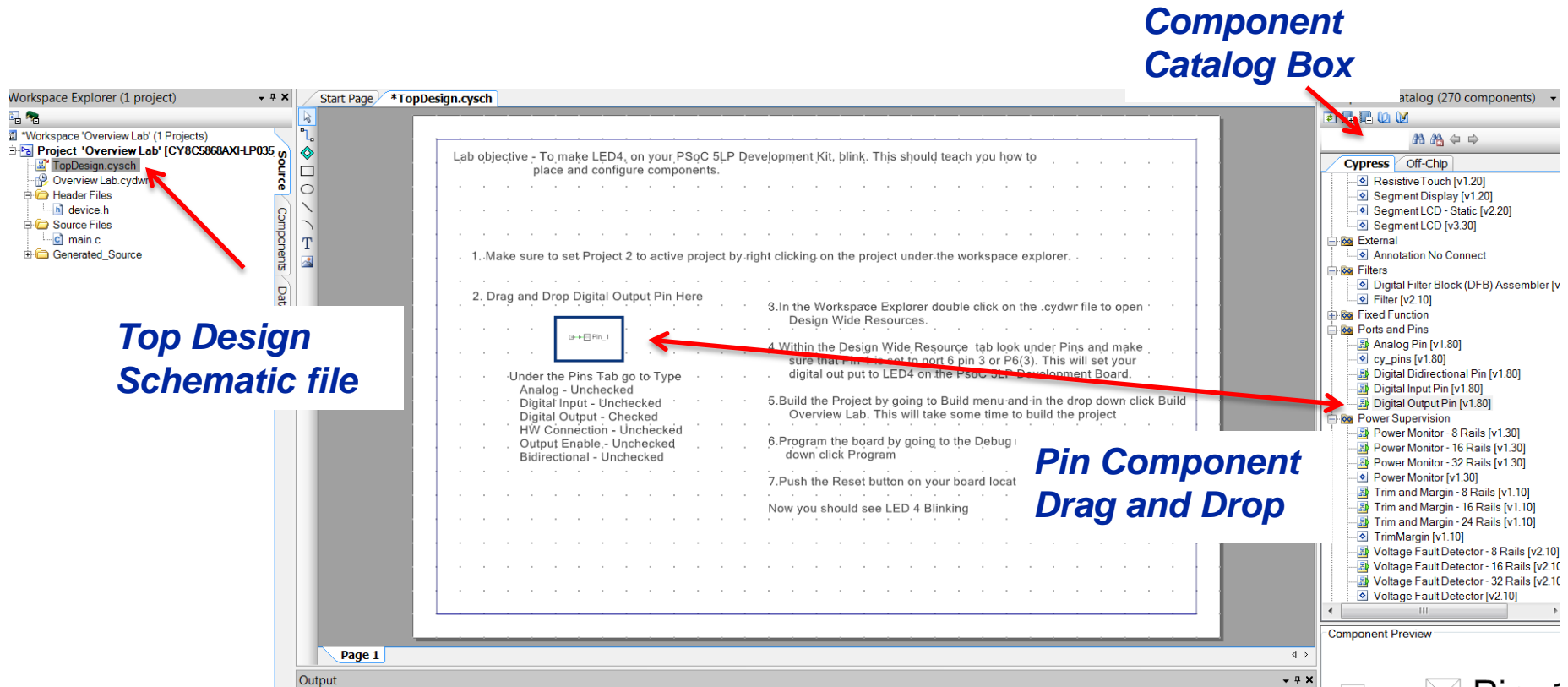
Architecture Overview Lab



1. Set Project as active project by right clicking on the project under the workspace explorer as shown. Project will then be highlighted in Bold.
2. Then, expand the “+” sign to the left of Project to view project files. Double-click the schematic file “TopDesign.cysch” to open it

Architecture Overview Lab

- From the “Component catalog” on the right side of the screen, drag & drop “Digital Output Pin” under “Ports and Pins” into the box (as shown below)



The screenshot displays the Cypress PSoC Designer workspace. On the left, the **Workspace Explorer** shows a project named "Project 'Overview Lab' (1 Projects)" with a file named "TopDesign.cysch". A red arrow points from the text "Top Design Schematic file" to this file. The main workspace area shows a schematic diagram with a grid. A red arrow points from the text "Pin Component Drag and Drop" to a box labeled "Pin 1" on the grid. On the right, the **Component Catalog** (labeled "Component Catalog Box" with a red arrow) lists various components. Under the "Ports and Pins" category, the "Digital Output Pin [v1.80]" component is highlighted with a red arrow. The catalog also shows other components like "Resistive Touch", "Segment Display", "Segment LCD", "Digital Filter Block (DFB) Assembler", "Analog Pin", "cy_pins", "Digital Bidirectional Pin", "Digital Input Pin", "Power Supervision", "Power Monitor", "Trim and Margin", "Voltage Fault Detector", and "TrimMargin".

Top Design Schematic file

Component Catalog Box

Pin Component Drag and Drop

4. Double-click the component to open it in configuration mode and check the configuration as follows:

Analog -
Unchecked

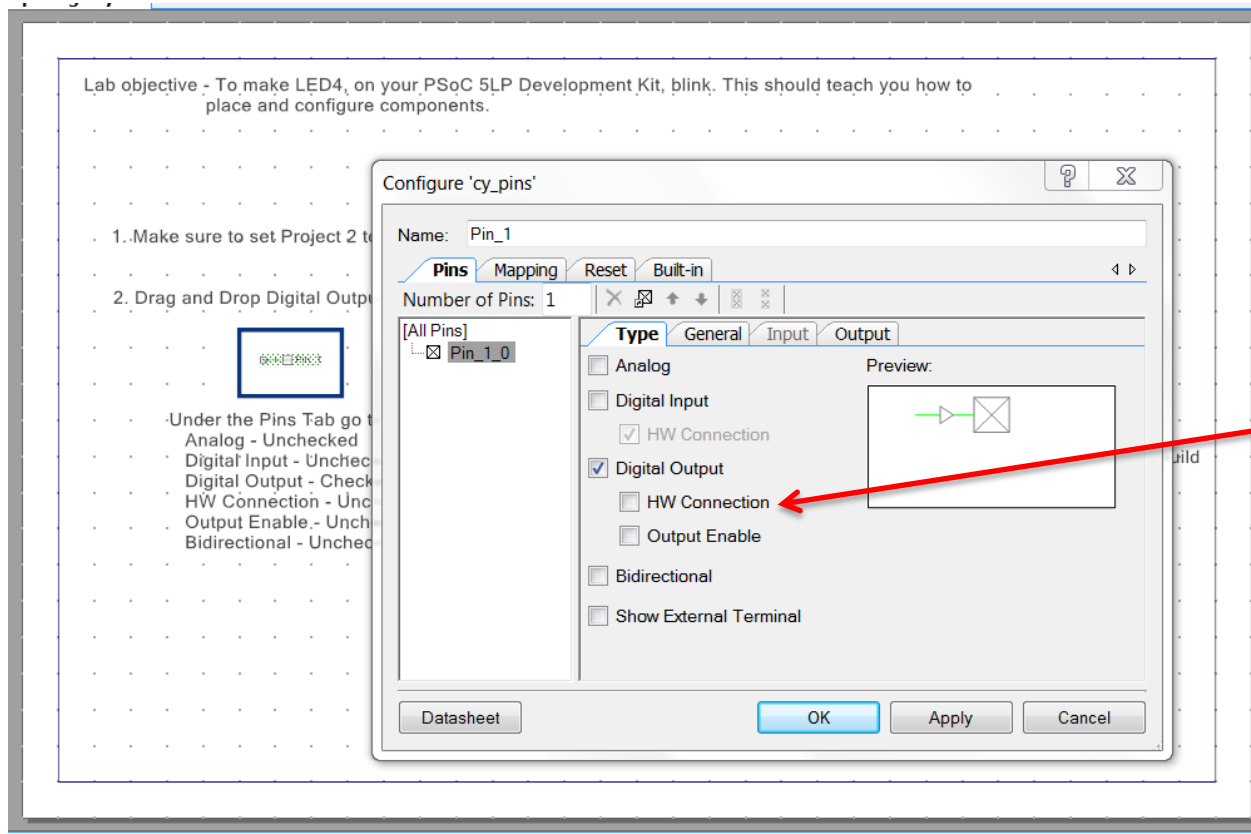
Digital Input –
Unchecked

Digital Output –
Checked

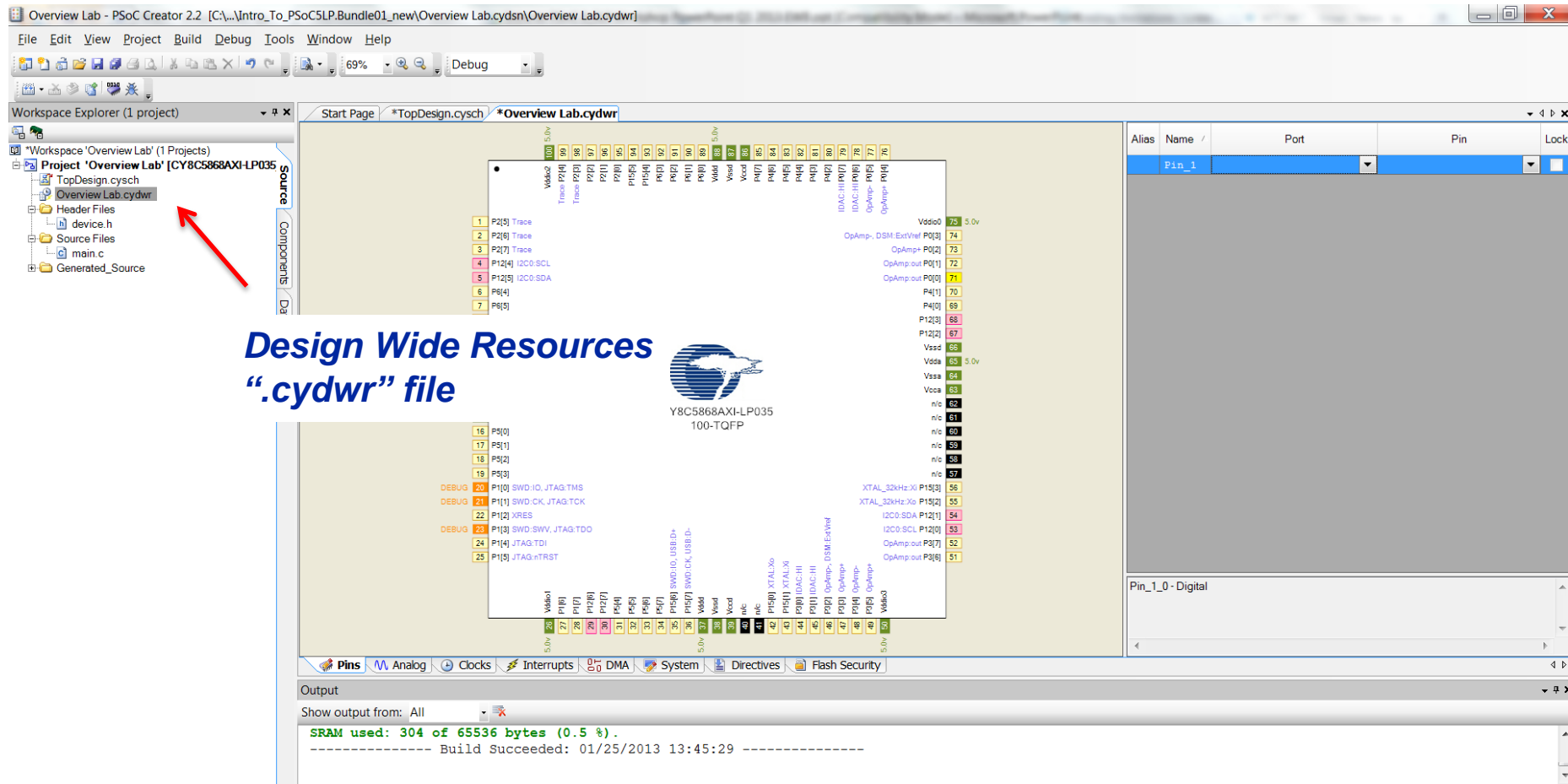
HW Connection –
Unchecked

Output Enable –
Unchecked

Bidirectional –
Unchecked



5. In the Workspace Explorer double click on the .cydwr file to open Design Wide Resources



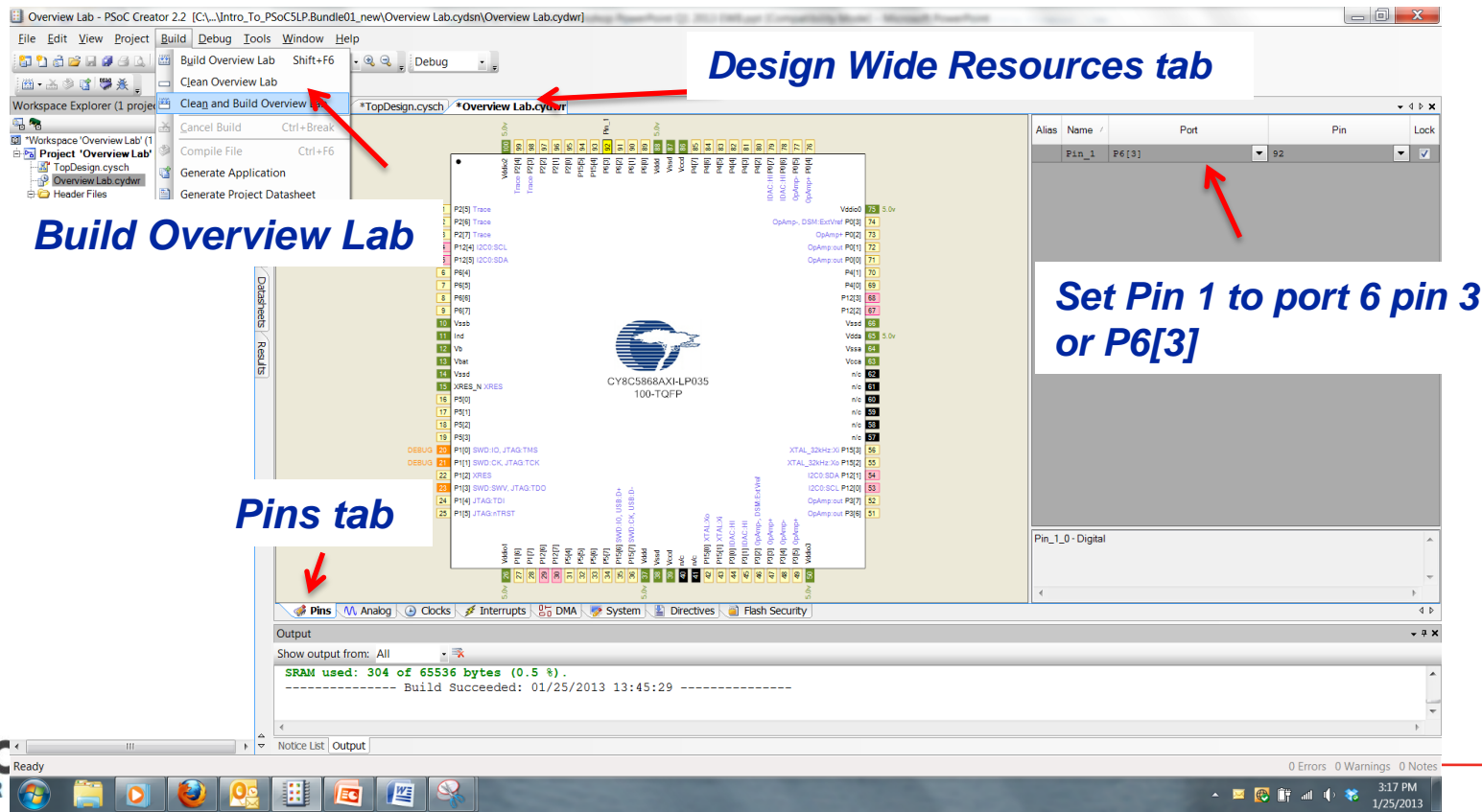
**Design Wide Resources
“.cydwr” file**

Alias	Name	Port	Pin	Lock
Pin_1				

SRAM used: 304 of 65536 bytes (0.5 %).
Build Succeeded: 01/25/2013 13:45:29

Architecture Overview Lab

6. Within the Design Wide Resources tab, select the Pins tab (below the chip)
7. On the right hand side of the screen, make sure that Pin 1 is set to port 6 pin 3 or P6[3]. This will set your digital output to LED4 on the PSoC Development Board.
8. Build the Project by going to the Build menu and in the drop down click "Build Overview Lab". This will take a minute to build the project.



Design Wide Resources tab

Build Overview Lab

Pins tab

Set Pin 1 to port 6 pin 3 or P6[3]

Alias	Name	Port	Pin	Lock
Pin_1	P6[3]	92		<input checked="" type="checkbox"/>

Output

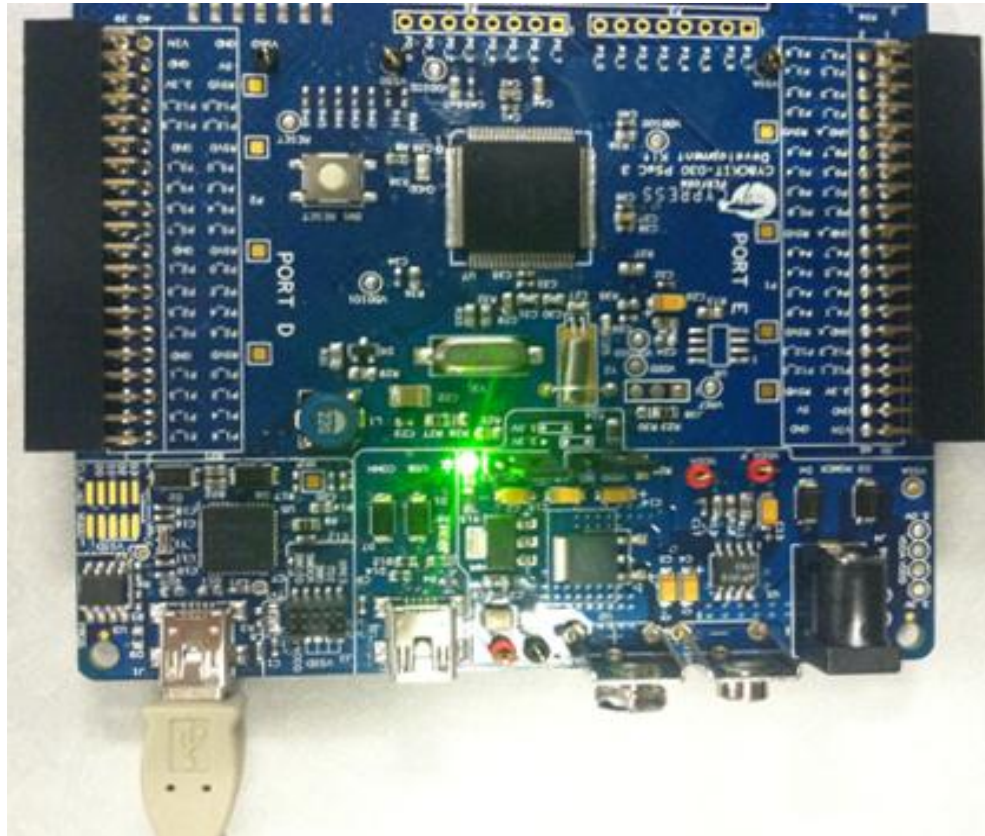
Show output from: All

SRAM used: 304 of 65536 bytes (0.5 %).

Build Succeeded: 01/25/2013 13:45:29

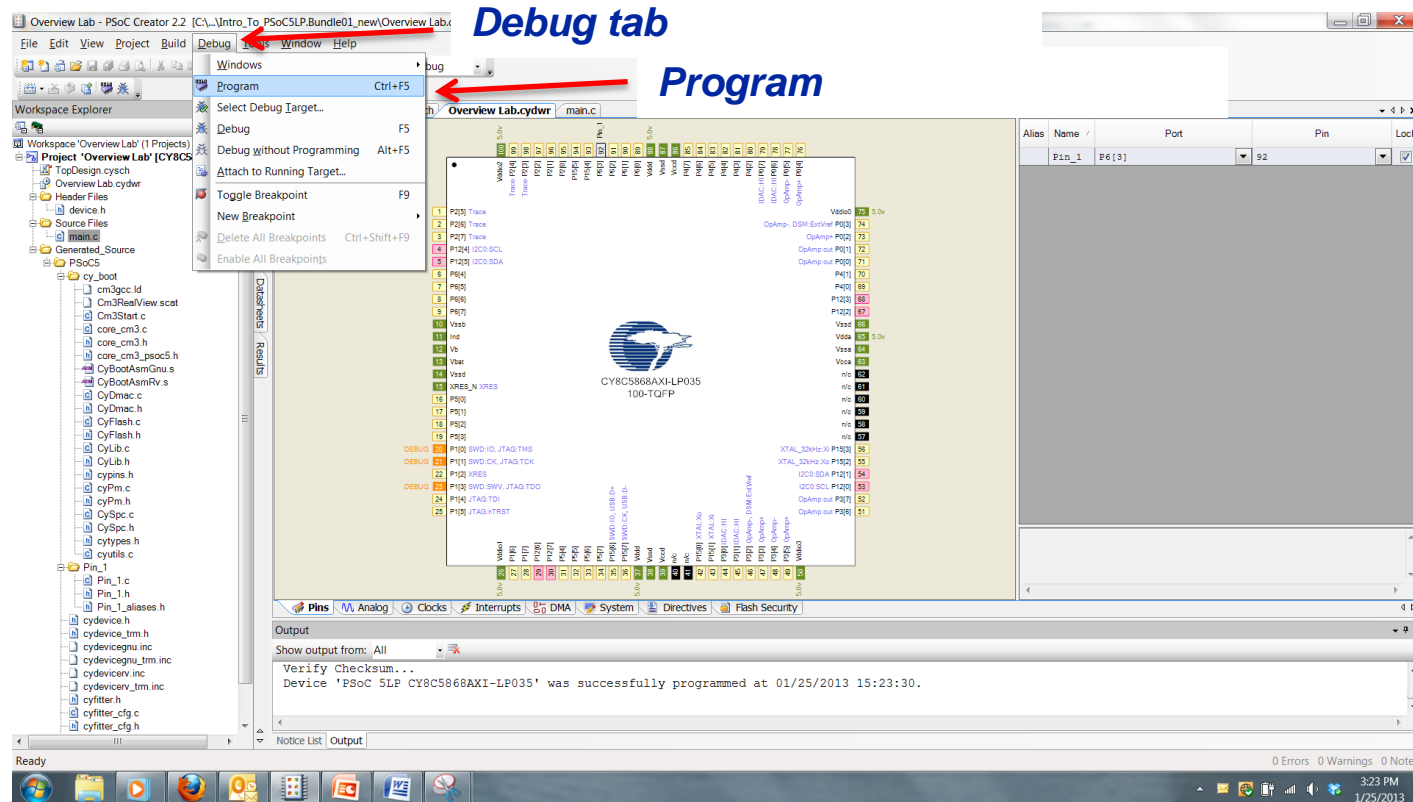
9. At this time, if you haven't already, plug in the USB cable from the kit (as shown in the picture below) into the board and plug in the other end into the computer.

If this is the first time that you are plugging in into the board, you may have to go through driver installation.



Architecture Overview Lab

10. Program the board by going to the Debug menu and click Program from the drop down list. Programming should take just a minute. You may have to select your kit and follow the steps to click on “Port Acquire”.
 11. Push the Reset button on your board located near Port D
- Verify that you see LED 4 Blinking.



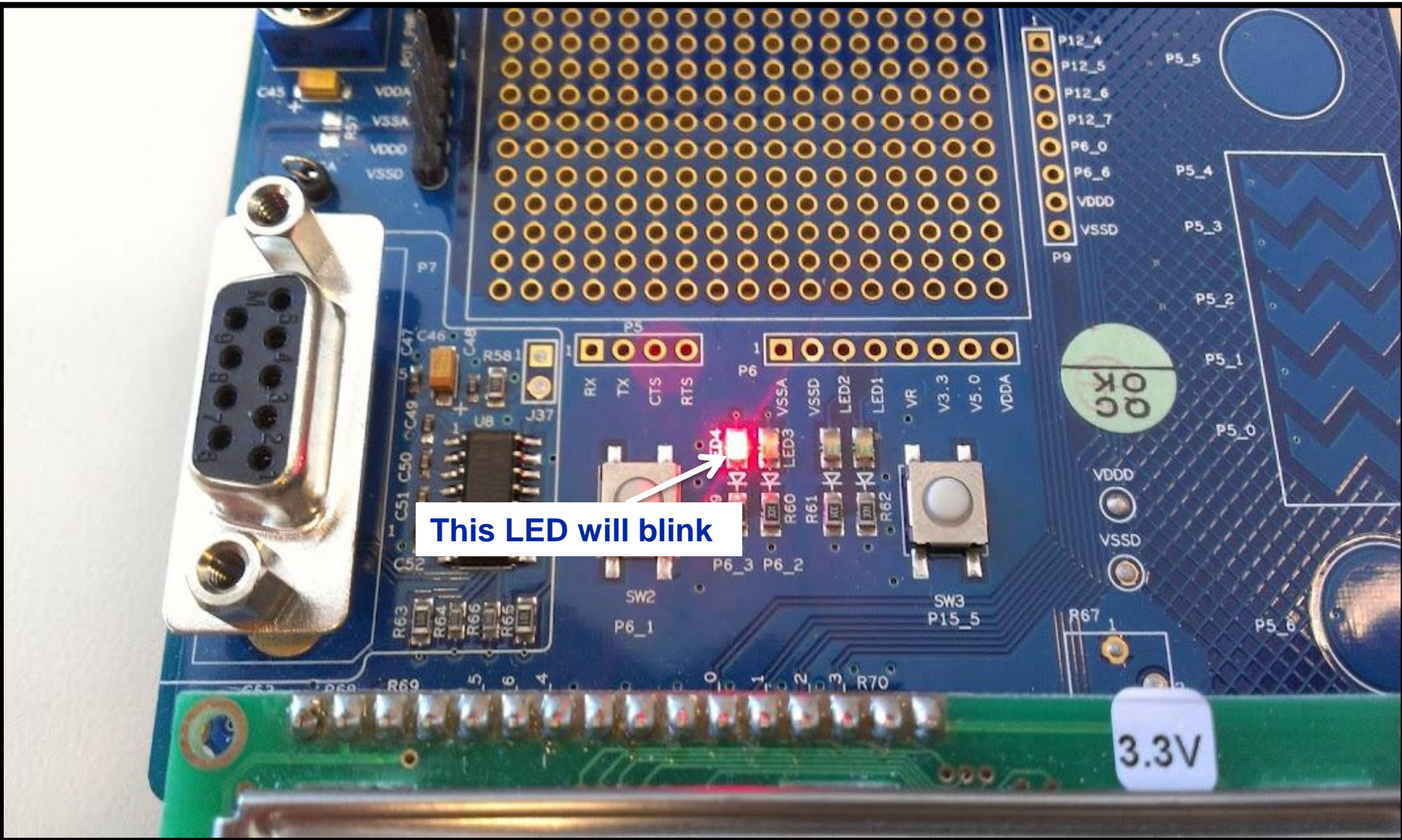
Debug tab

Program

Output:

```
Verify Checksum...
Device 'PSoC SLP CY8C5868AXI-LP035' was successfully programmed at 01/25/2013 15:23:30.
```


Architecture Overview Lab



INTRODUCTION TO PSOC 3 AND PSOC 5LP

DIGITAL PERIPHERALS

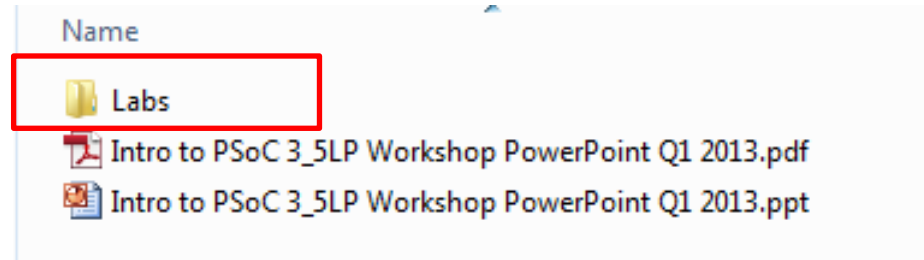
LAB- LAB 1

Lab Objective

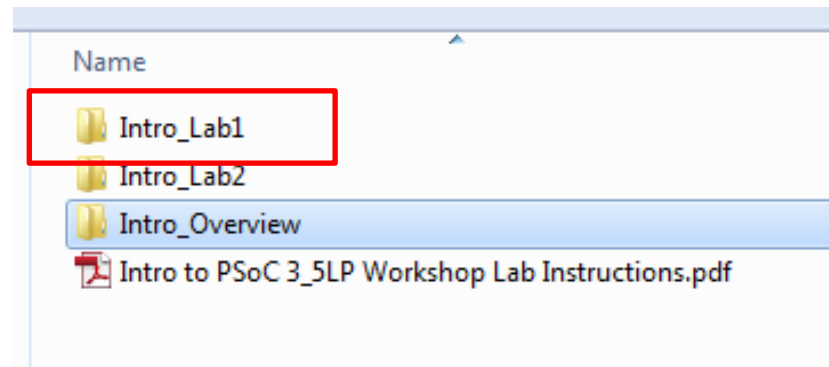
- Make LED3 & LED4 on your PSoC Development Kit blink
- Learn how to place and configure components in PSoC Creator
- Understand the System on Chip Capability of PSoC
- LED3 will blink using two PWMs to change the duty cycle on the LED to make it a “Breathing” LED
- LED4 will blink via software control

Lab 1

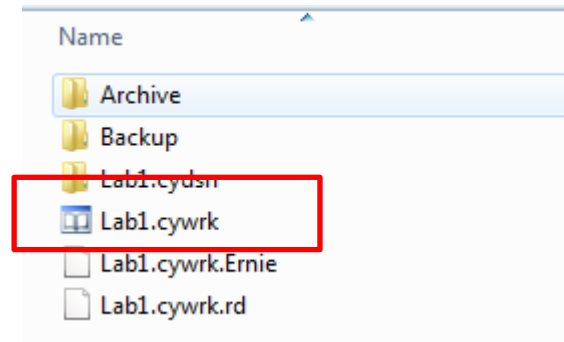
- Open Labs Directory



- Open Intro_Lab1 Directory


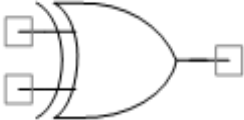
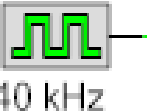
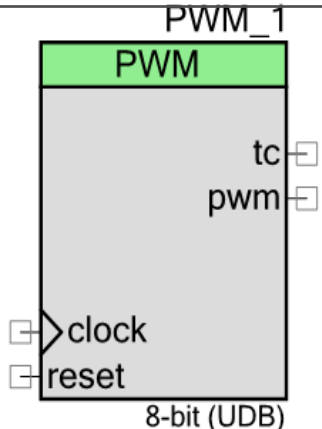



- Double Click 'Lab1.cywrk'



Lab 1

1. The Software LED has already been configured for you.
Follow the instructions below to complete the rest of the design
2. Find the following components found in the Component catalog on the right side of the screen and place them in the boxes given on the “Top Design.cysch” schematic file under Lab_1. Be sure to only place 1 PWM. Components are shown below:

Logic Low '0'		XOR Gate	
Clock	Clock_1 	PWM	
Digital Output Pin			

3. Place the components inside the right boxes shown on the schematic file
4. Double click on the clock component to open it in configuration mode and set it to 40 kHz
5. Double click on the PWM component to open it in configuration mode and make the following changes to its properties

Set Properties to:

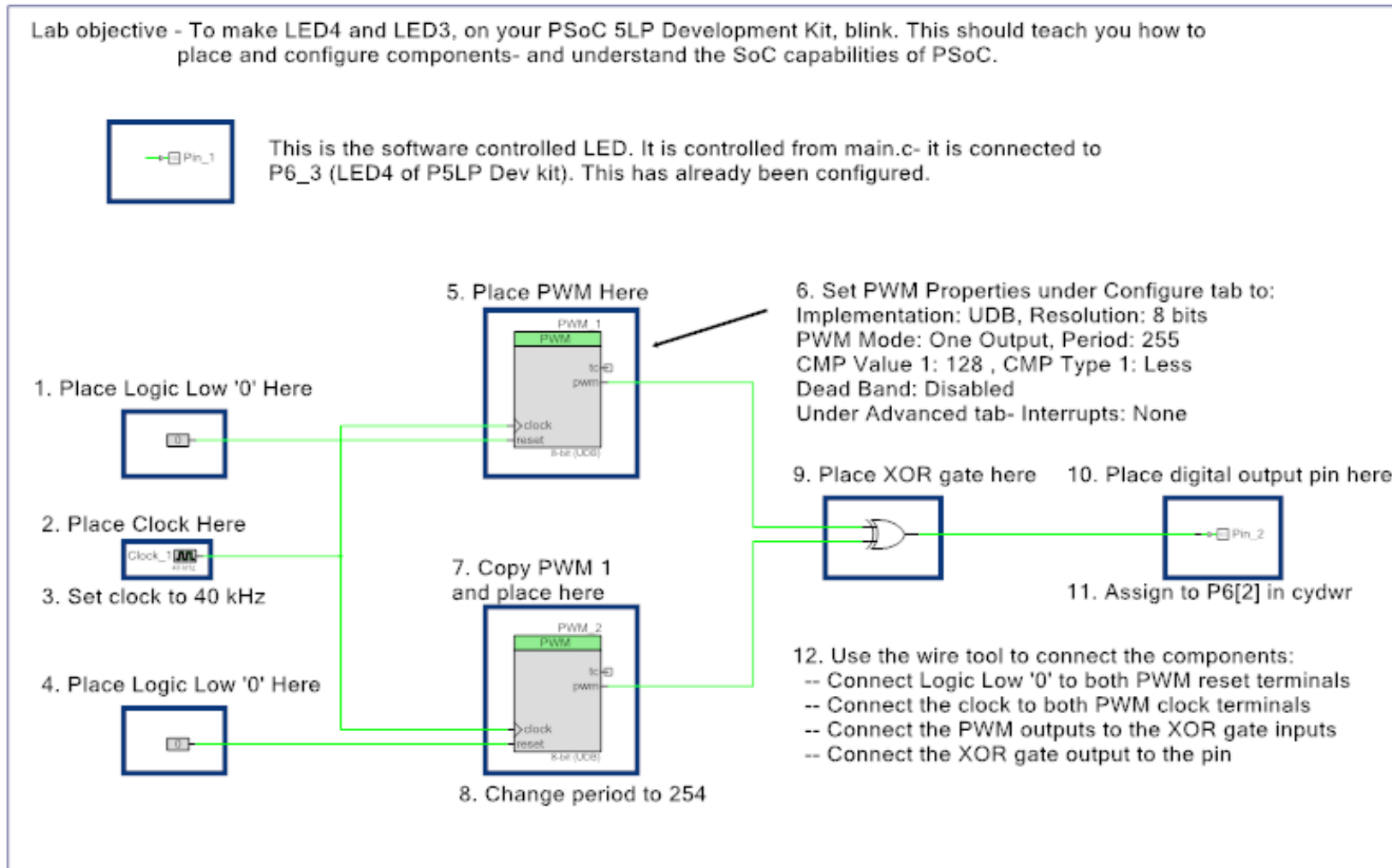
Implementation: UDB	CMP Value 1: 128
Resolution: 8-Bits	CMP Type 1: Less
PWM mode: One Output	Dead Band : Disabled*
Period: 255	Under Advanced tab:* Interrupts: None

6. Copy the first PWM from the top box into the bottom box and change the "Period" to 254

*You may need to expand the customizer window to expose these settings

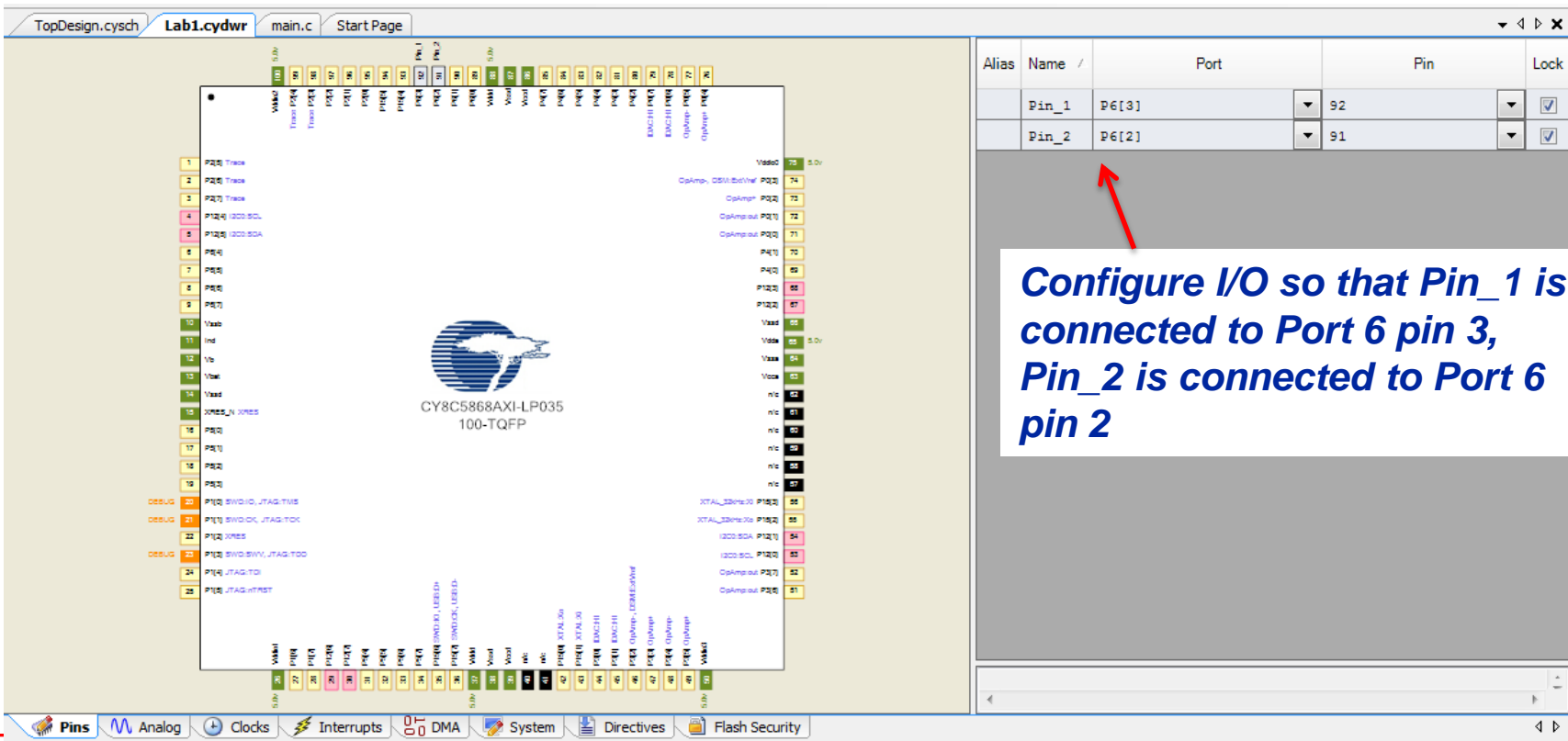
7. Use the wire tool to make the following connections between the components:
- Connect Logic Low '0' to PWM reset terminals
 - Connect the clock to both PWM clock terminals
 - Connect the PWM outputs to the XOR gate inputs
 - Connect the XOR gate output to the pin.

8. Your final schematic should look like this when complete



Lab 1

9. In the Workspace Explorer double click on the .cydwr file to open Design wide Resources
10. In the Design wide Resources tab locate the section for pins on the right
11. Configure the I/O so that Pin 1 is connected to Port 6 pin 3 or P6[3], Pin 2 is connected to Port 6 pin 2 or P6[2]..



Alias	Name /	Port	Pin	Lock
Pin_1		P6[3]	92	<input checked="" type="checkbox"/>
Pin_2		P6[2]	91	<input checked="" type="checkbox"/>

Configure I/O so that Pin_1 is connected to Port 6 pin 3, Pin_2 is connected to Port 6 pin 2

12. Build the project by going to the Build menu selecting Build Digital Peripherals Lab or pressing Shift + F6. This will take some time to build the project.
13. Program the board by going to the Debug menu and in the drop down click Program
14. Push the Reset button on your board located near Port D

Verify: LED 4 is blinking and LED3 is “Breathing”.

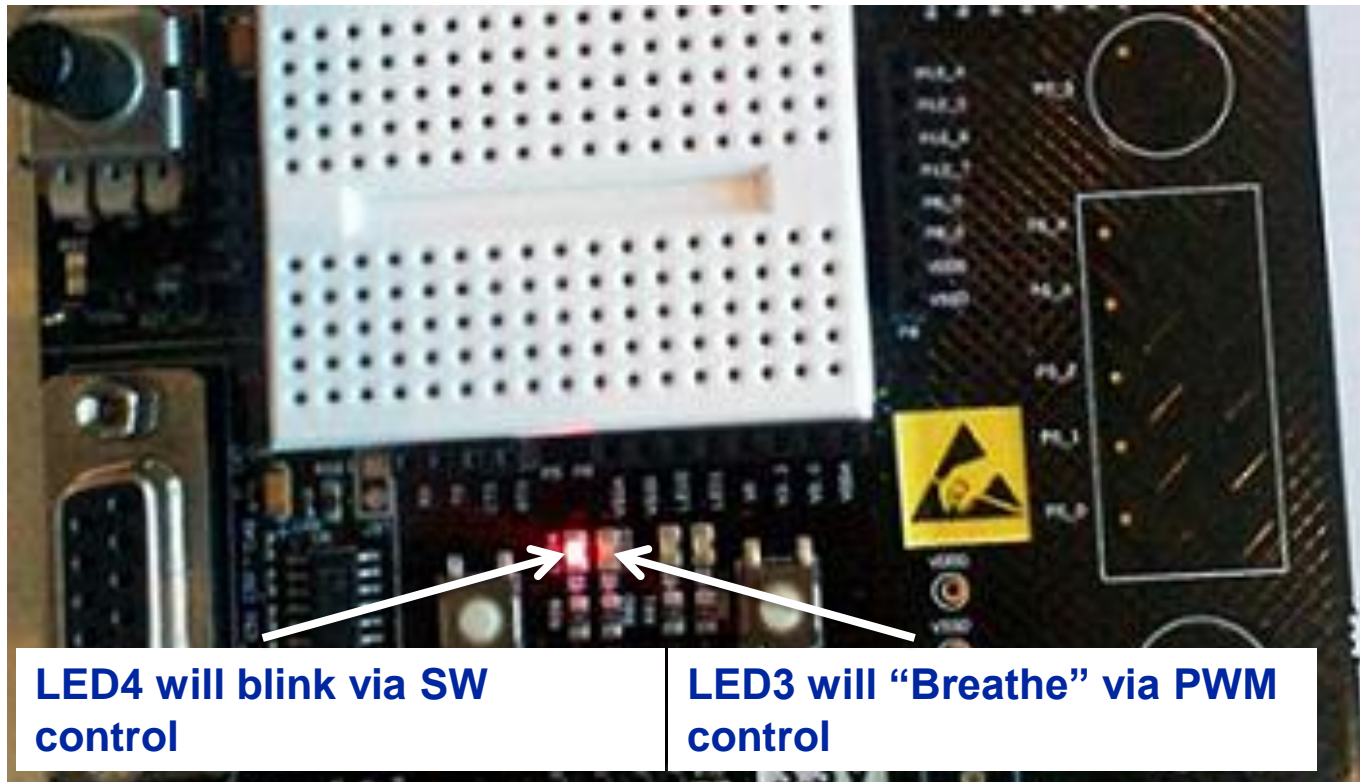
15. Re-program the board by going to the Debug and selecting Debug.
16. Start the program by clicking on the green arrow in the tool bar



17. Allow to run then halt execution-



Validate that LED4 has stopped blinking, LED3 continues to 'Breathe'. Why?



INTRODUCTION TO PSOC 3 AND PSOC 5LP

ANALOG PERIPHERALS

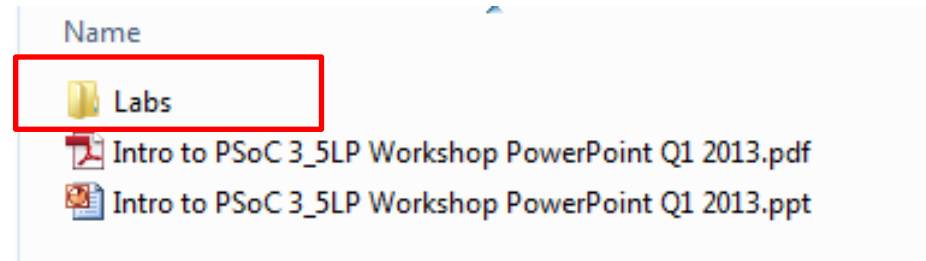
LAB- LAB 2

Lab Objective

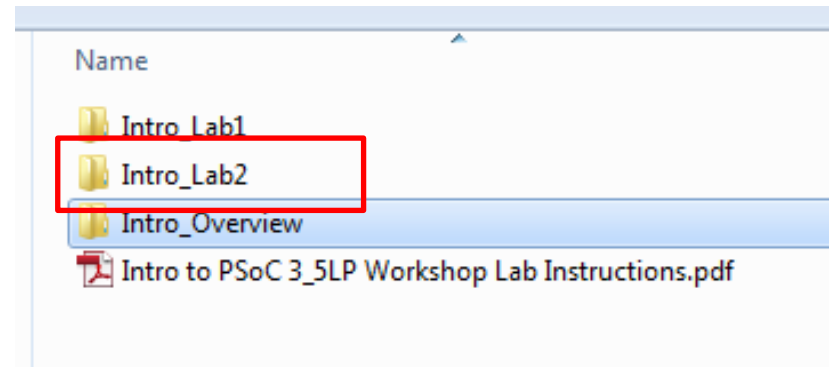
- To convert an output from the potentiometer into a digital number using the ADC
- To display the digital number on the LCD Screen on PSoC Development Kit

Lab 2

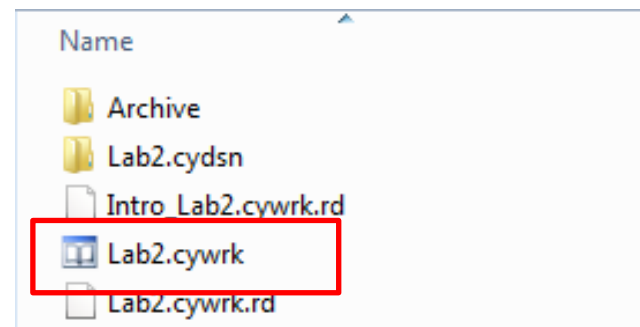
- Open Labs Directory



- Open Intro_Lab2 Directory

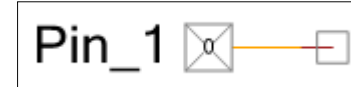


- Double Click 'Lab2.cywrk'



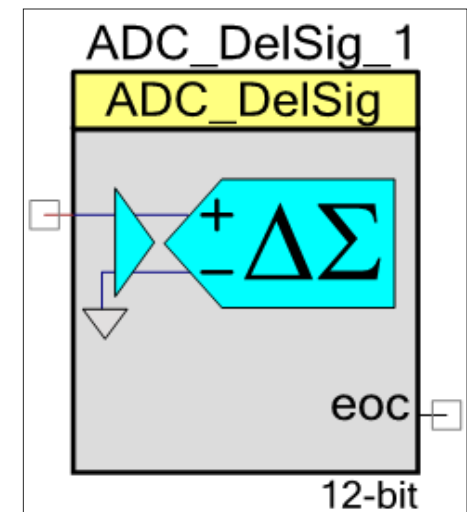
Instructions:

1. Place the Analog Pin from Component Catalog as shown here in the adjacent box
2. Place the Delta Sigma ADC in the box as shown below.
3. Double-click on the component to open it in the configuration mode and make the following changes:



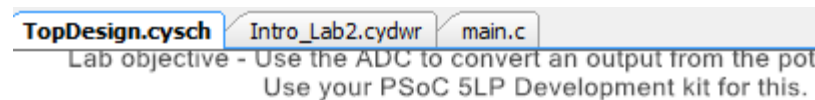
Set Properties to:

Conversion Mode: 1-Multi Sample	Input Mode: Single
Resolution: 12-Bits	Input Range: Vssa to Vdda
Conversion Rate: 1000 SPS	Buffer Gain: 1
Clock Frequency: 131 kHz (Calculated value)	Buffer Mode: Rail to Rail



Lab 2

4. Use the wire tool found on the left side of the worksheet (shown in slide 23) to connect Pin 1 to the ADC input. To use the wire tool hover over the connections until an 'X' appears, then click to make the connection.
5. Your final schematic should look like this when complete



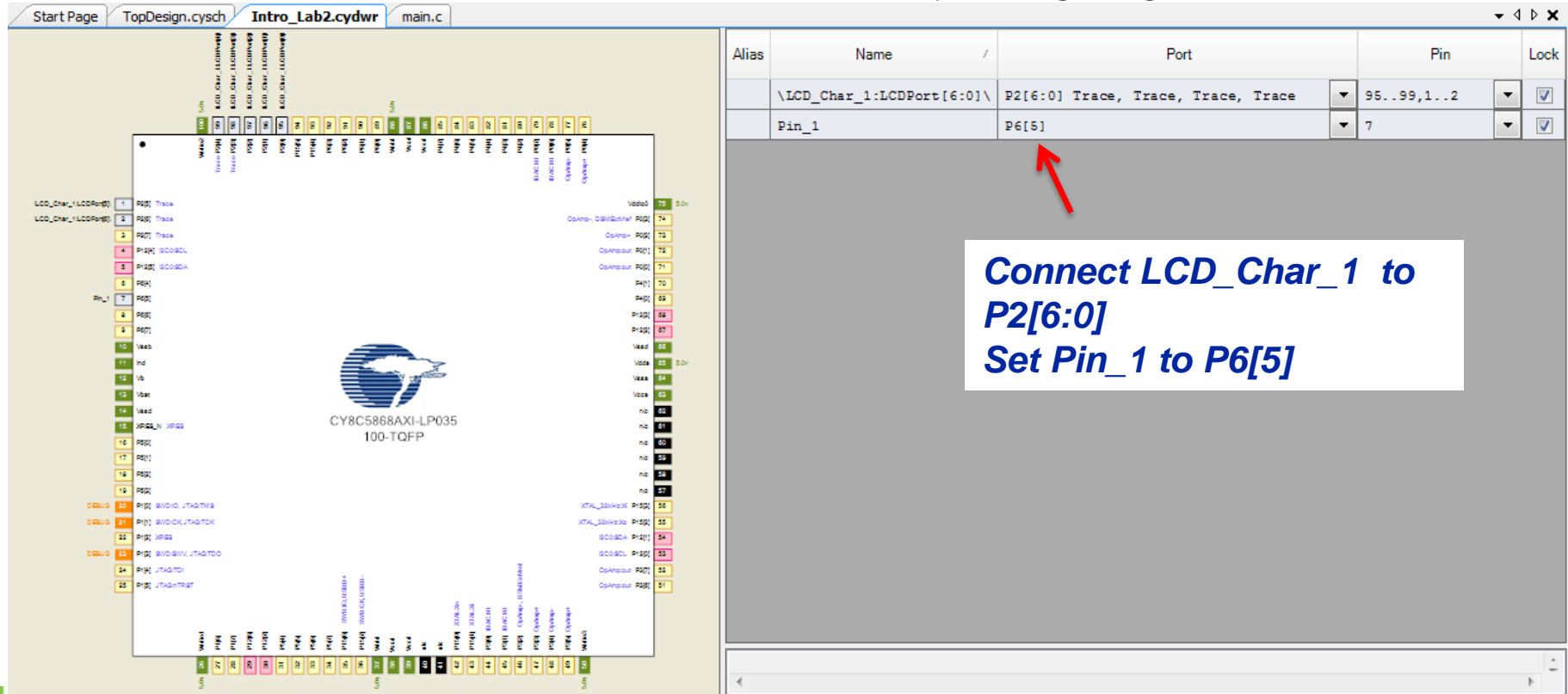
1. Place Analog Pin Here 2. Place Delta Sigma ADC Here



Set Properties to:

- Conversion Mode: 1-Multi Sample
- Resolution: 12-Bits
- Conversion Rate: 1000 SPS
- Clock Frequency: 131 kHz
(Calculated value)
- Input Mode: Single
- Input Range: Vssa to Vdda
- Buffer Gain: 1
- Buffer Mode: Rail to Rail

6. In the Workspace Explorer double click on the .cydwr file to open Design wide Resources (as explained in Overview lab)
7. In the Design wide Resources tab locate the section for pins on the right
8. Connect the LCD to Port 2 by assigning LCDPort[6:0] to P2[6:0]. Connect Pin 1 to the potentiometer (Port 6, Pin 5) by assigning Pin_1 to P6(5).



The screenshot shows the Cypress PSoC Designer workspace. The main window displays the pin configuration table for the CY8C5868AXI-LP035 100-TQFP. The table has columns for Alias, Name, Port, Pin, and Lock. A red arrow points to the Pin_1 entry in the table, which is assigned to P6[5]. A callout box with blue text provides instructions: "Connect LCD_Char_1 to P2[6:0]" and "Set Pin_1 to P6[5]".

Alias	Name	Port	Pin	Lock
\LCD_Char_1:LCDPort[6:0]	P2[6:0] Trace, Trace, Trace, Trace	95..99,1..2	<input checked="" type="checkbox"/>	
Pin_1	P6[5]	7	<input checked="" type="checkbox"/>	

**Connect LCD_Char_1 to P2[6:0]
Set Pin_1 to P6[5]**

9. Build the project by going to the Build menu selecting Build System Resources Lab. This will take some time to build the project.
10. At this point, verify that the board is plugged in.
11. Program the board by going to the Debug menu and in the drop down click Program
12. Push the Reset button on your board located near Port D
13. Verify: When you turn the POT you should see the ADC values change

Lab 2

