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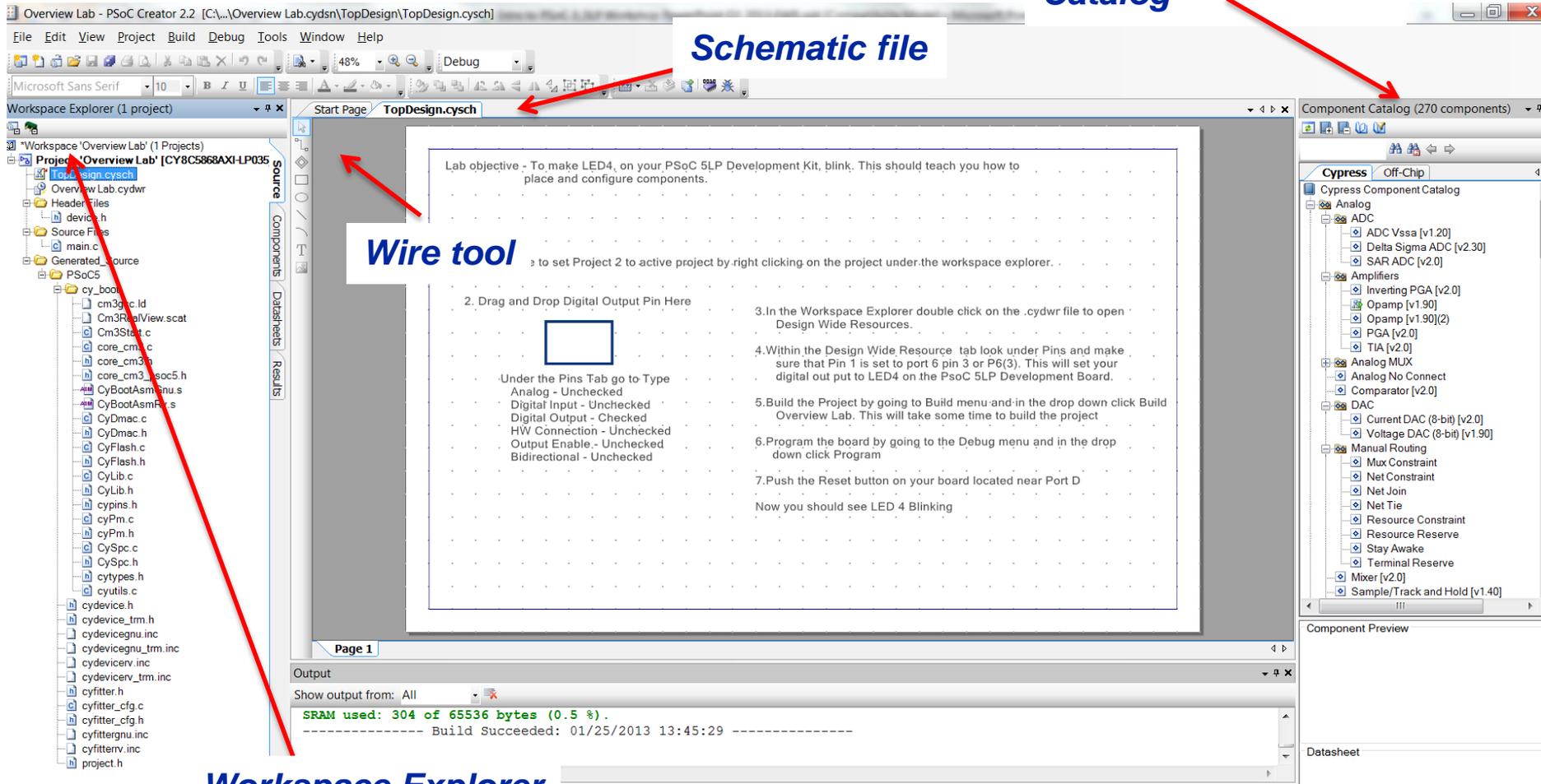
INTRODUCTION TO PSOC 3 AND PSOC 5LP

# ARCHITECTURE OVERVIEW

# LAB - WALKTHROUGH

# PSoC Creator 2.2 Interface

Cypress Component  
Catalog



The screenshot displays the PSoC Creator 2.2 interface. The **Workspace Explorer** on the left shows a project tree with files like `cm3g.c`, `cm3ra`, and `cm3st`. The **Schematic file** in the center contains a lab objective and a list of pin configurations: Analog - Unchecked, Digital Input - Unchecked, Digital Output - Checked, HW Connection - Unchecked, Output Enable - Unchecked, and Bidirectional - Unchecked. The **Component Catalog** on the right lists various components such as ADC, Amplifiers, Analog MUX, DAC, and Manual Routing. The **Output** window at the bottom shows the build result: `SRAM used: 304 of 65536 bytes (0.5 %)` and `Build Succeeded: 01/25/2013 13:45:29`. Red arrows point to the **Wire tool** icon in the schematic editor and the **Component Catalog** window.

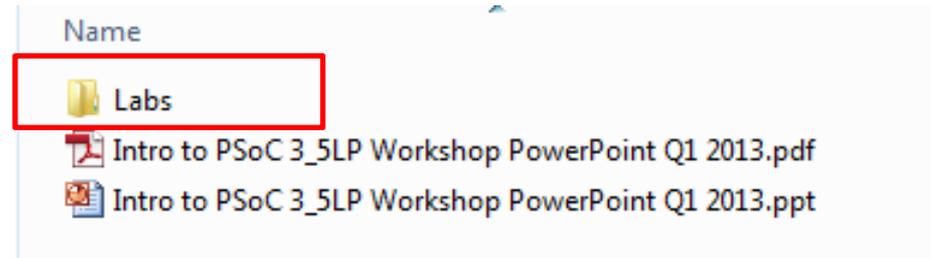
Workspace Explorer

## Lab Objective

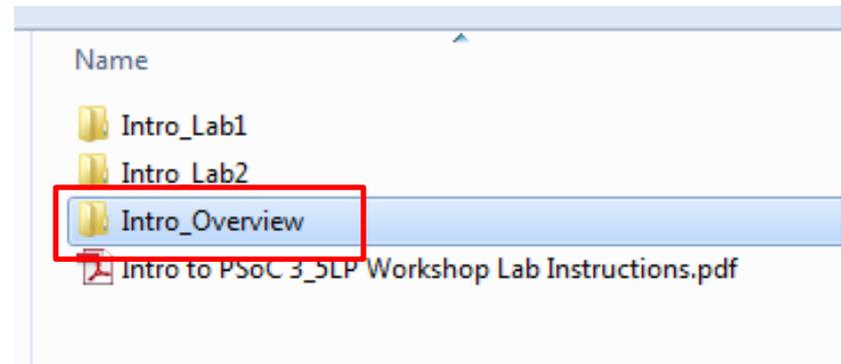
- To make LED4 on your PSoC Development Kit blink.
- To learn how to place and configure components in PSoC Creator

# Architecture Overview Lab

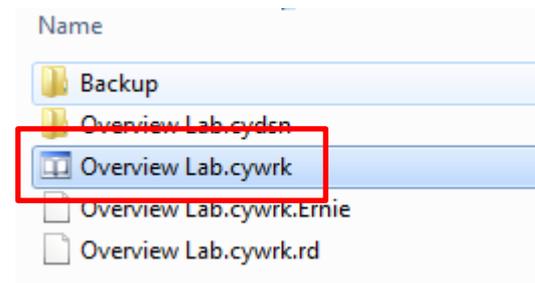
- Open Labs Directory



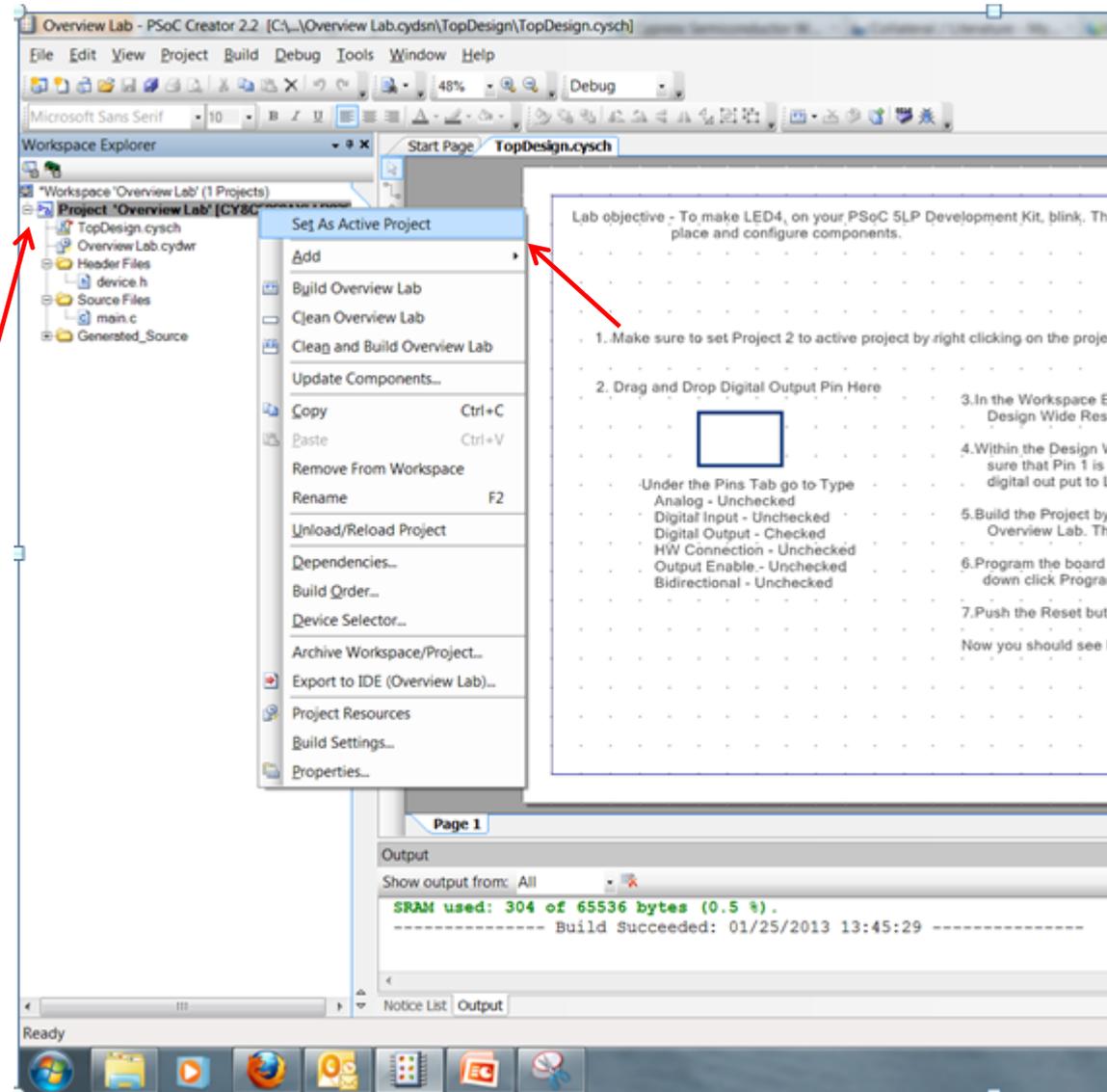
- Open Intro\_Overview Directory



- Double Click 'Overview Lab.cywrk'



# Architecture Overview Lab

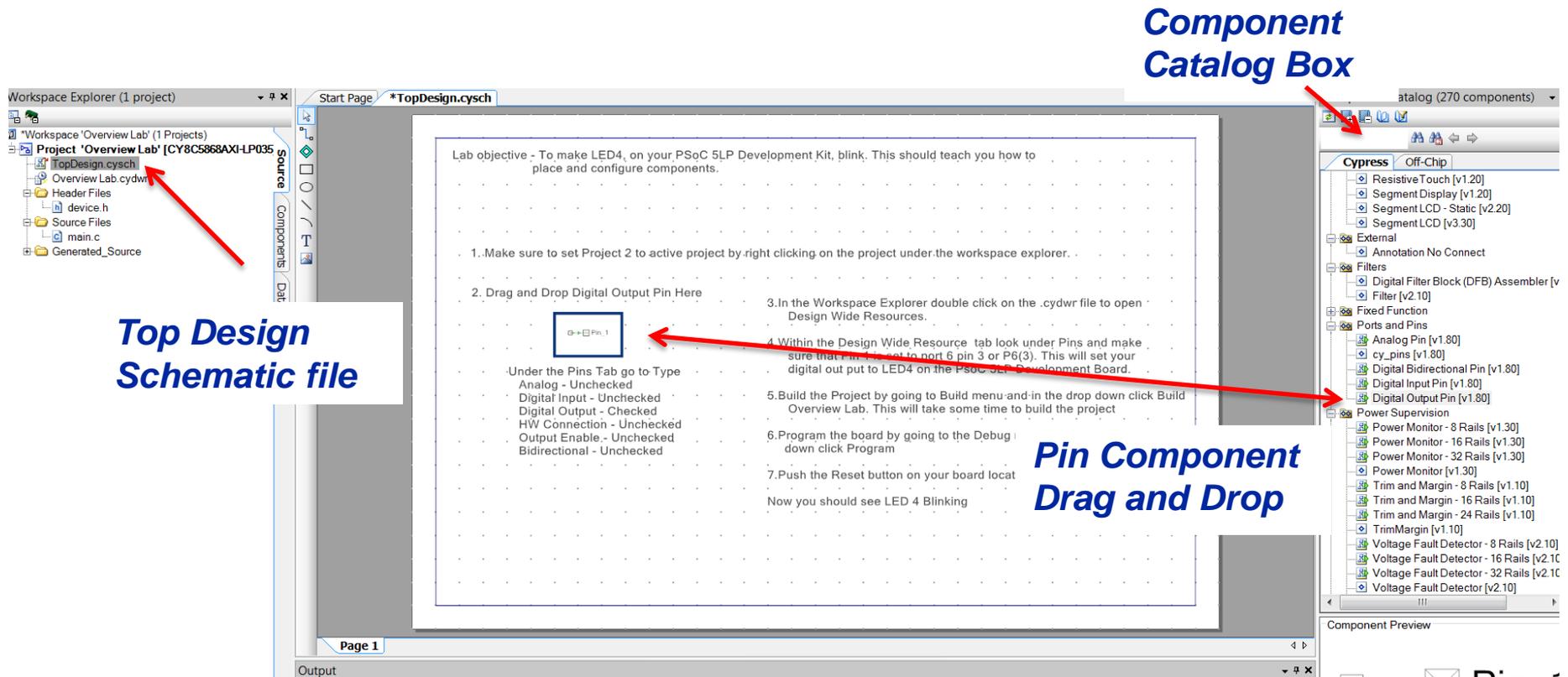


1. Set Project as active project by right clicking on the project under the workspace explorer as shown. Project will then be highlighted in Bold.

2. Then, expand the “+” sign to the left of Project to view project files. Double-click the schematic file “TopDesign.cysch” to open it

# Architecture Overview Lab

- From the “Component catalog” on the right side of the screen, drag & drop “Digital Output Pin” under “Ports and Pins” into the box (as shown below)



**Component Catalog Box**

**Top Design Schematic file**

**Pin Component Drag and Drop**

Workspace Explorer (1 project) | Start Page | \*TopDesign.cysch | Component Catalog (270 components)

Project 'Overview Lab' [CY8C5868AXI-LP035]

TopDesign.cysch

Overview Lab.cydwr

Header Files

device.h

Source Files

main.c

Generated\_Source

Lab objective - To make LED4, on your PSoC 5LP Development Kit, blink. This should teach you how to place and configure components.

- Make sure to set Project 2 to active project by right clicking on the project under the workspace explorer.
- Drag and Drop Digital Output Pin Here
- In the Workspace Explorer double click on the .cydwr file to open Design Wide Resources.
- Within the Design Wide Resource tab look under Pins and make sure that pin 4 is set to port 6 pin 3 or P6(3). This will set your digital output to LED4 on the PSoC 5LP Development Board.
- Build the Project by going to Build menu and in the drop down click Build Overview Lab. This will take some time to build the project
- Program the board by going to the Debug menu and in the drop down click Program
- Push the Reset button on your board located on the board

Now you should see LED 4 Blinking

Under the Pins Tab go to Type

- Analog - Unchecked
- Digital Input - Unchecked
- Digital Output - Checked
- HW Connection - Unchecked
- Output Enable - Unchecked
- Bidirectional - Unchecked

Component Catalog (270 components)

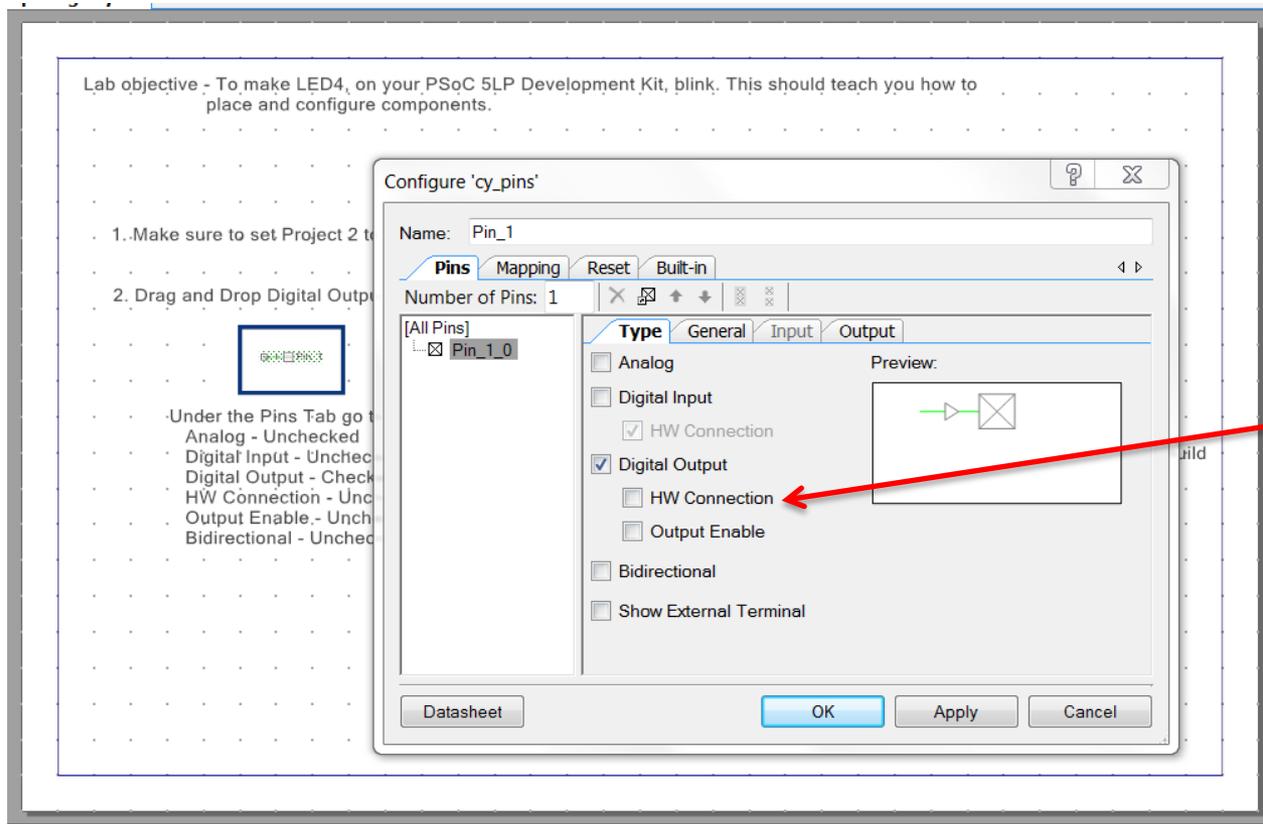
Cypress Off-Chip

- Resistive Touch [v1.20]
- Segment Display [v1.20]
- Segment LCD - Static [v2.20]
- Segment LCD [v3.30]
- External
  - Annotation No Connect
- Filters
  - Digital Filter Block (DFB) Assembler [v1.10]
  - Filter [v2.10]
- Fixed Function
- Ports and Pins
  - Analog Pin [v1.80]
  - cy\_pins [v1.80]
  - Digital Bidirectional Pin [v1.80]
  - Digital Input Pin [v1.80]
  - Digital Output Pin [v1.80]
- Power Supervision
  - Power Monitor - 8 Rails [v1.30]
  - Power Monitor - 16 Rails [v1.30]
  - Power Monitor - 32 Rails [v1.30]
  - Power Monitor [v1.30]
  - Trim and Margin - 8 Rails [v1.10]
  - Trim and Margin - 16 Rails [v1.10]
  - Trim and Margin - 24 Rails [v1.10]
  - TrimMargin [v1.10]
  - Voltage Fault Detector - 8 Rails [v2.10]
  - Voltage Fault Detector - 16 Rails [v2.10]
  - Voltage Fault Detector - 32 Rails [v2.10]
  - Voltage Fault Detector [v2.10]

Component Preview

4. Double-click the component to open it in configuration mode and check the configuration as follows:

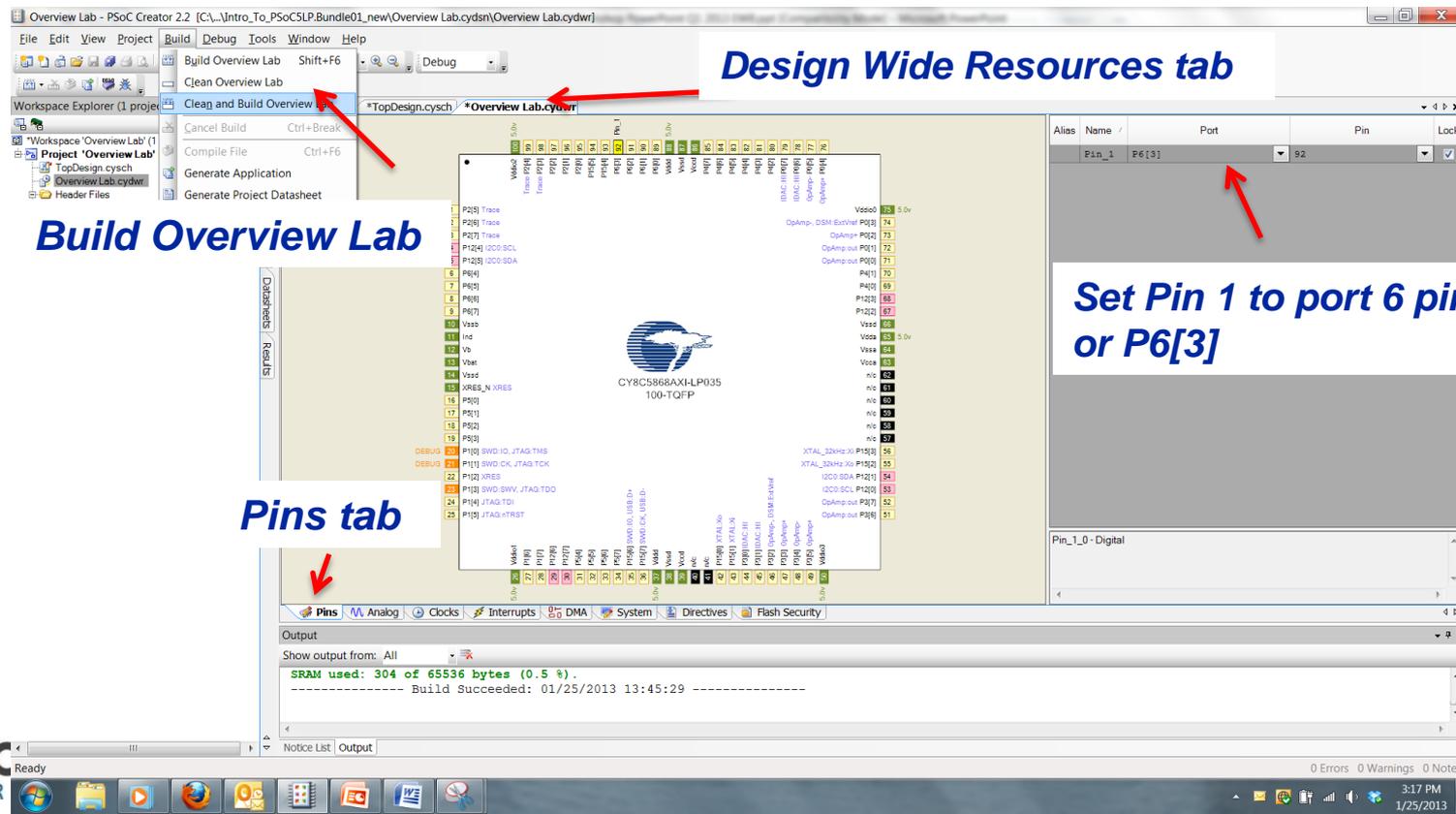
- Analog -**  
Unchecked
- Digital Input –**  
Unchecked
- Digital Output –**  
Checked
- HW Connection –**  
Unchecked
- Output Enable –**  
Unchecked
- Bidirectional –**  
Unchecked





# Architecture Overview Lab

6. Within the Design Wide Resources tab, select the Pins tab (below the chip)
7. On the right hand side of the screen, make sure that Pin 1 is set to port 6 pin 3 or P6[3]. This will set your digital output to LED4 on the PSoC Development Board.
8. Build the Project by going to the Build menu and in the drop down click “Build Overview Lab”. This will take a minute to build the project.



**Design Wide Resources tab**

**Build Overview Lab**

**Pins tab**

**Set Pin 1 to port 6 pin 3 or P6[3]**

Alias	Name	Port	Pin	Lock
Pin_1	P6[3]		92	<input checked="" type="checkbox"/>

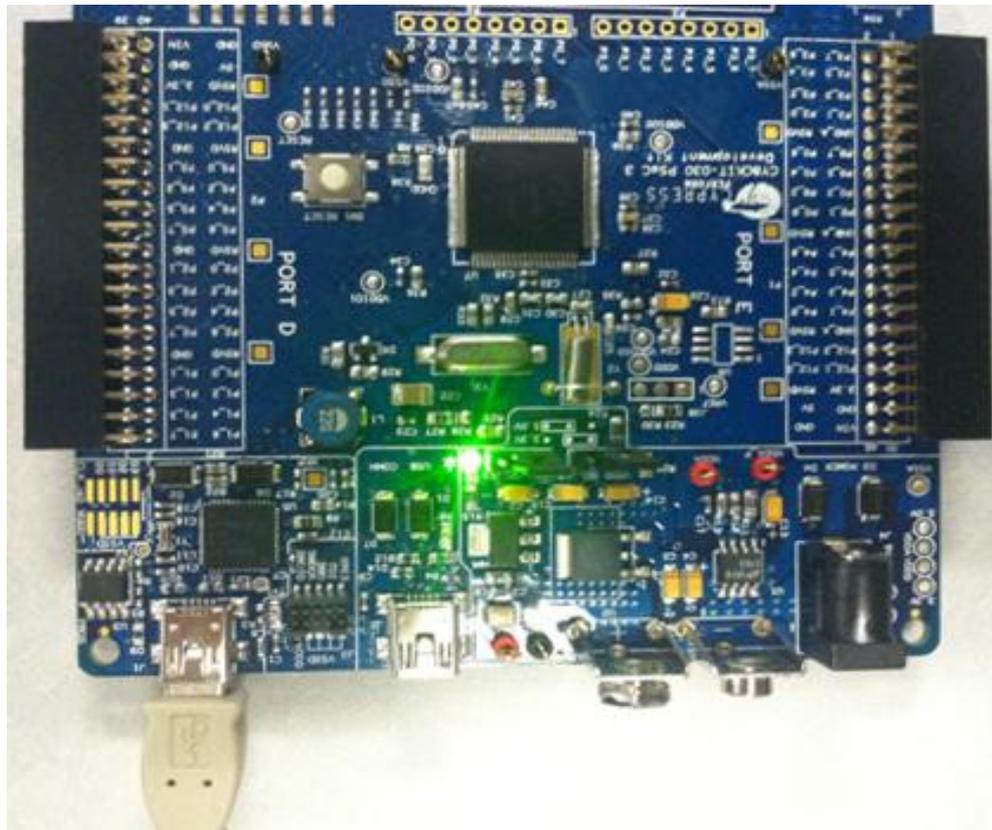
Output

Show output from: All

```
SRAM used: 304 of 65536 bytes (0.5 %).  
----- Build Succeeded: 01/25/2013 13:45:29 -----
```

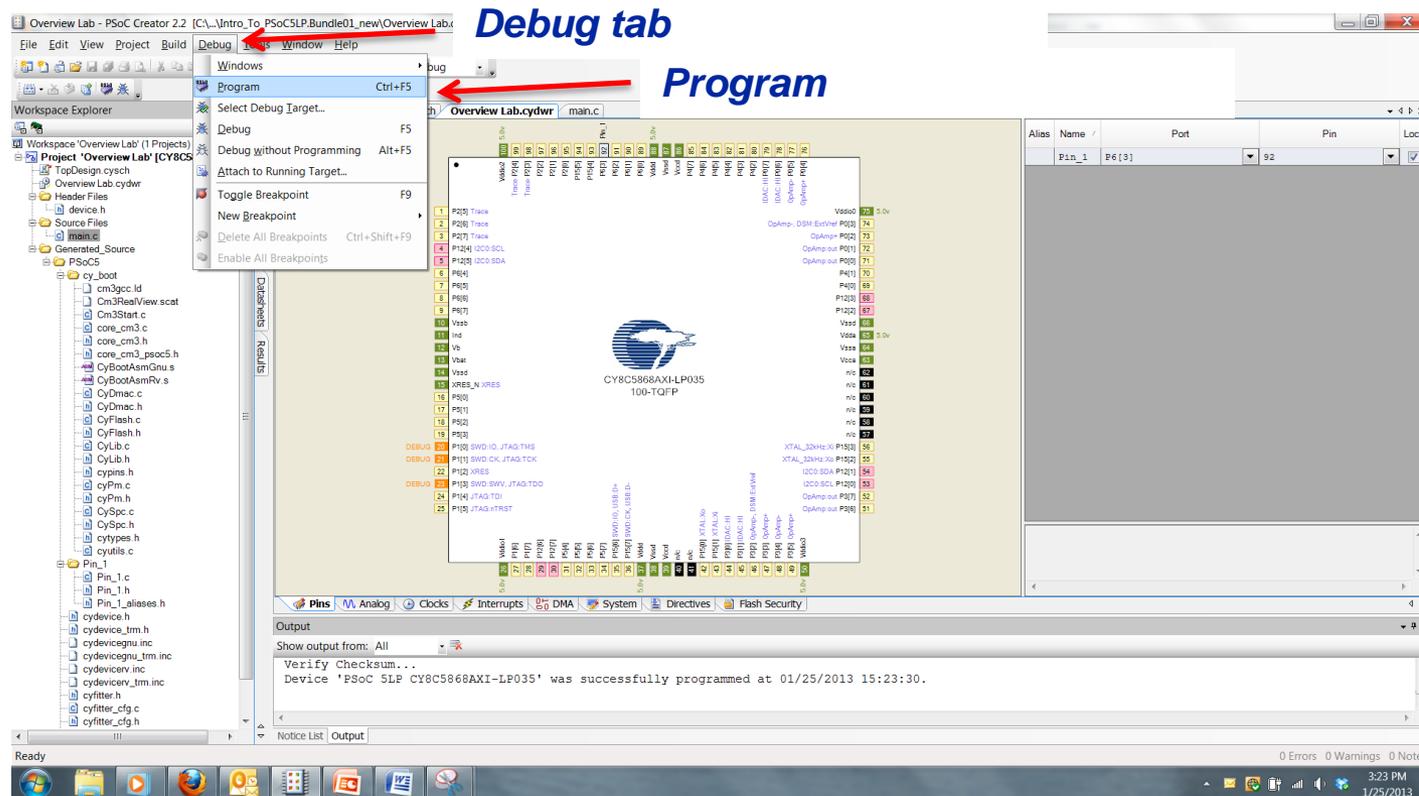
9. At this time, if you haven't already, plug in the USB cable from the kit (as shown in the picture below) into the board and plug in the other end into the computer.

If this is the first time that you are plugging in into the board, you may have to go through driver installation.



# Architecture Overview Lab

10. Program the board by going to the Debug menu and click Program from the drop down list. Programming should take just a minute. You may have to select your kit and follow the steps to click on “Port Acquire”.
  11. Push the Reset button on your board located near Port D
- Verify that you see LED 4 Blinking.



**Debug tab**

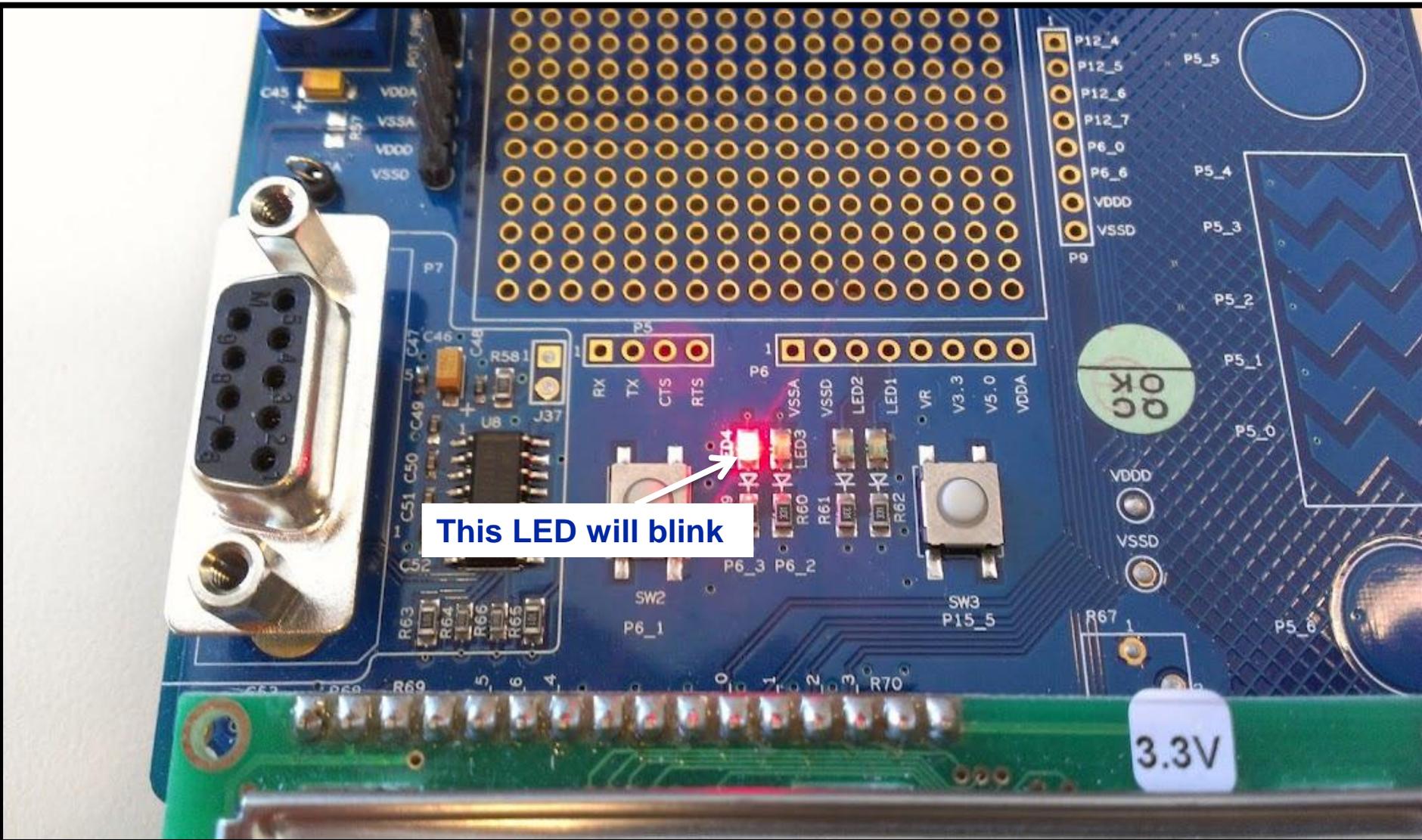
**Program**

Alias	Name	Port	Pin	Lock
Pin_1	P6(3)		92	<input checked="" type="checkbox"/>

Output

```
Show output from: All
Verify Checksum...
Device 'PSoC SLP CY8C5868AXI-LP035' was successfully programmed at 01/25/2013 15:23:30.
```

# Architecture Overview Lab



This LED will blink

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INTRODUCTION TO PSOC 3 AND PSOC 5LP

# DIGITAL PERIPHERALS

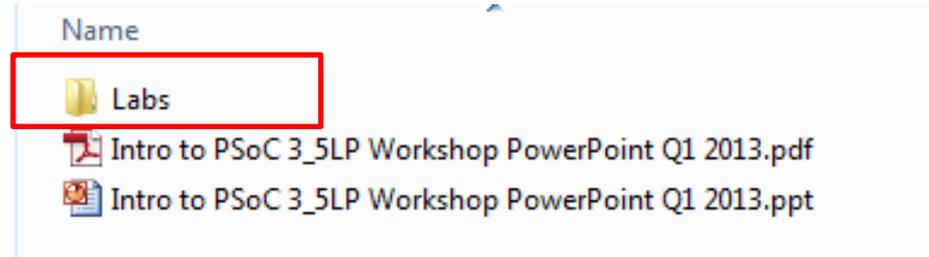
## LAB- LAB 1

## Lab Objective

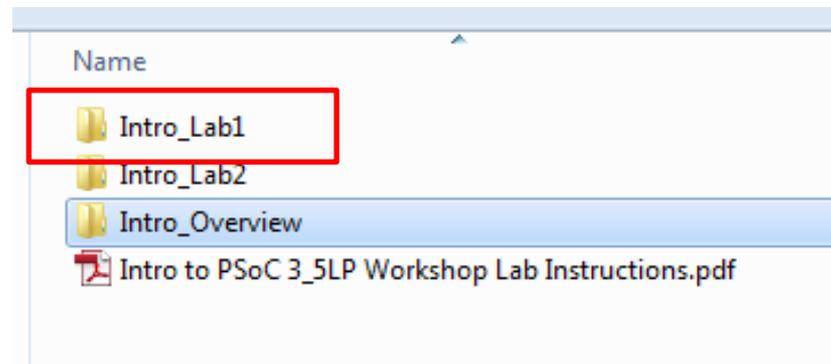
- Make LED3 & LED4 on your PSoC Development Kit blink
- Learn how to place and configure components in PSoC Creator
- Understand the System on Chip Capability of PSoC
- LED3 will blink using two PWMs to change the duty cycle on the LED to make it a “Breathing” LED
- LED4 will blink via software control

# Lab 1

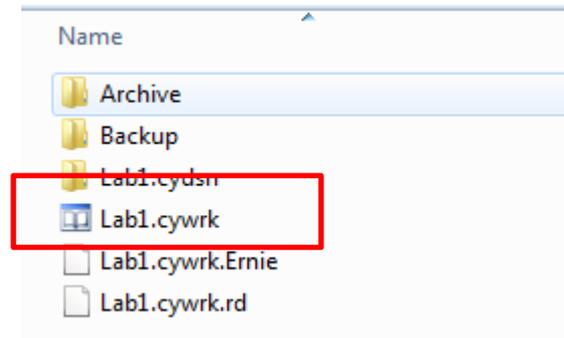
- Open Labs Directory



- Open Intro\_Lab1 Directory

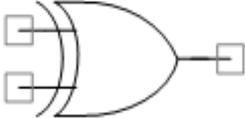
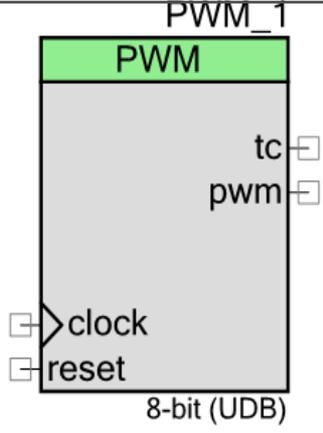


- Double Click 'Lab1.cywrk'



# Lab 1

1. The Software LED has already been configured for you.  
Follow the instructions below to complete the rest of the design
2. Find the following components found in the Component catalog on the right side of the screen and place them in the boxes given on the “Top Design.cysch” schematic file under Lab\_1. Be sure to only place 1 PWM. Components are shown below:

<p>Logic Low '0'</p> 	<p>XOR Gate</p> 
<p>Clock</p> <p>Clock_1 </p>	<p>PWM</p> 
<p>Digital Output Pin</p> 	

3. Place the components inside the right boxes shown on the schematic file
4. Double click on the clock component to open it in configuration mode and set it to 40 kHz
5. Double click on the PWM component to open it in configuration mode and make the following changes to its properties

## Set Properties to:

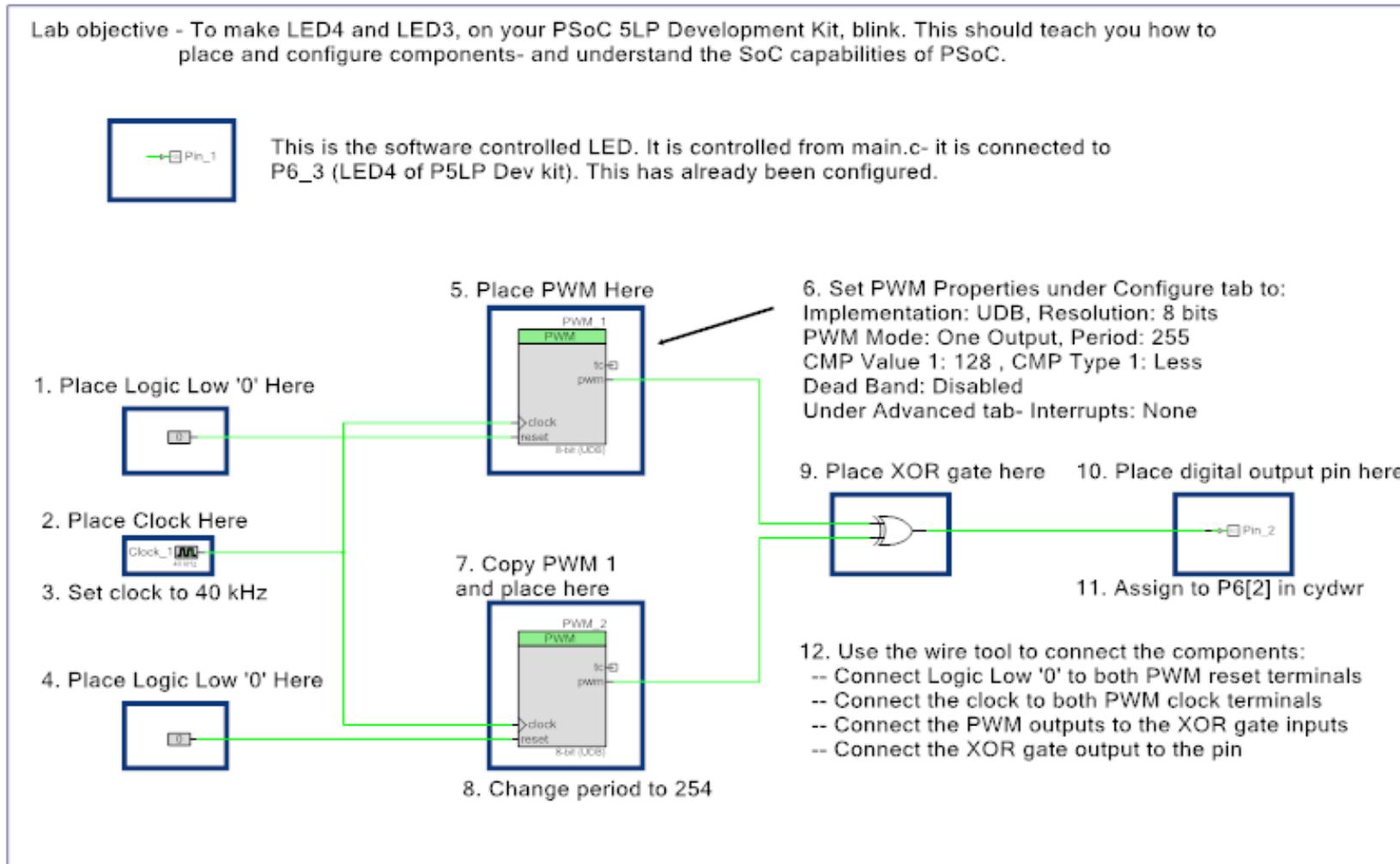
Implementation: UDB	CMP Value 1: 128
Resolution: 8-Bits	CMP Type 1: Less
PWM mode: One Output	Dead Band : Disabled*
Period: 255	Under Advanced tab:* Interrupts: None

6. Copy the first PWM from the top box into the bottom box and change the "Period" to 254

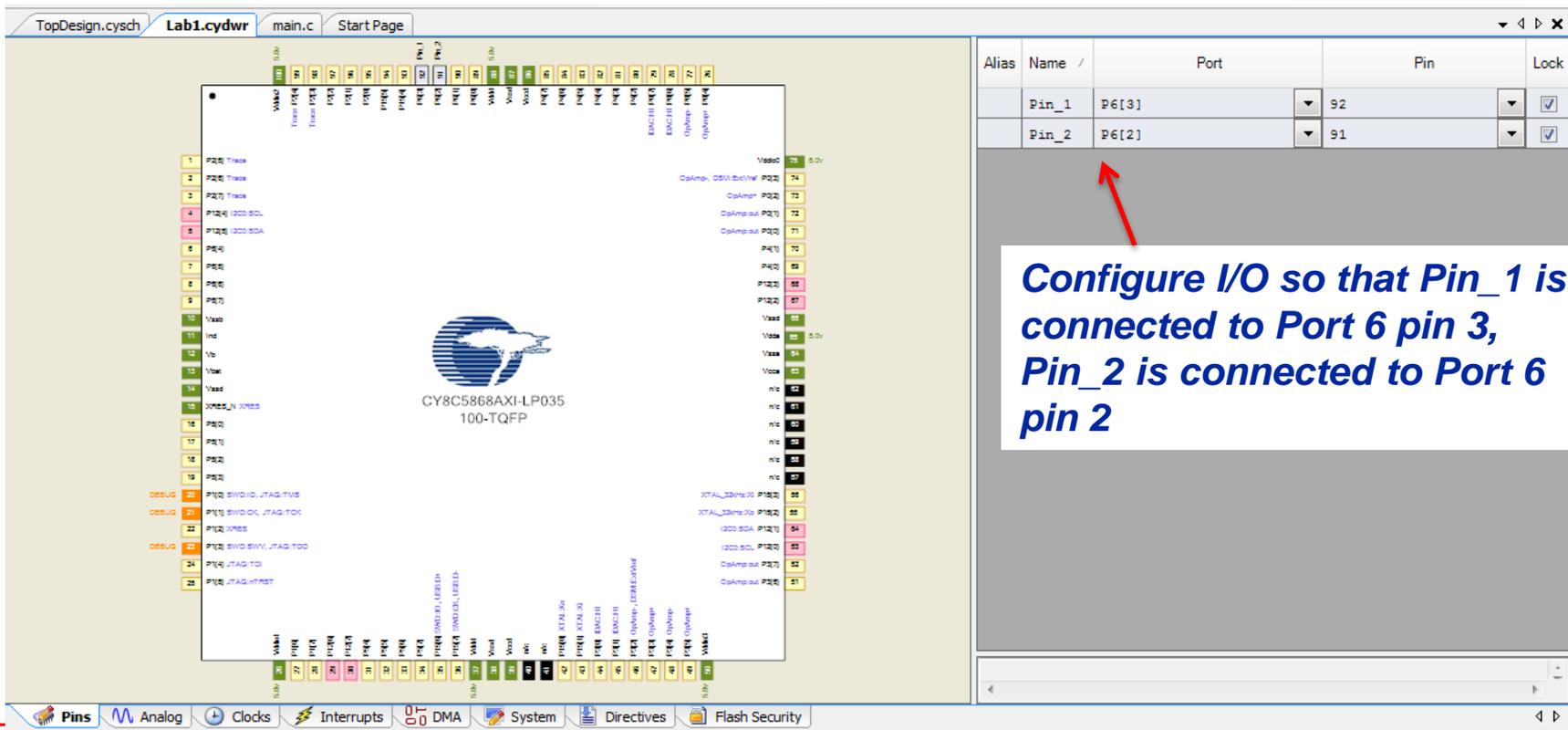
\*You may need to expand the customizer window to expose these settings

7. Use the wire tool to make the following connections between the components:
  - Connect Logic Low '0' to PWM reset terminals
  - Connect the clock to both PWM clock terminals
  - Connect the PWM outputs to the XOR gate inputs
  - Connect the XOR gate output to the pin.

## 8. Your final schematic should look like this when complete



9. In the Workspace Explorer double click on the .cydwr file to open Design wide Resources
10. In the Design wide Resources tab locate the section for pins on the right
11. Configure the I/O so that Pin 1 is connected to Port 6 pin 3 or P6[3], Pin 2 is connected to Port 6 pin 2 or P6[2]..



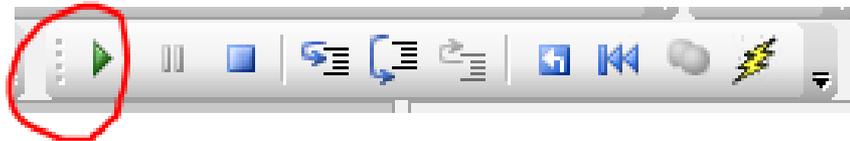
Alias	Name /	Port	Pin	Lock
Pin_1		P6[3]	92	<input checked="" type="checkbox"/>
Pin_2		P6[2]	91	<input checked="" type="checkbox"/>

**Configure I/O so that Pin\_1 is connected to Port 6 pin 3, Pin\_2 is connected to Port 6 pin 2**

12. Build the project by going to the Build menu selecting Build Digital Peripherals Lab or pressing Shift + F6. This will take some time to build the project.
13. Program the board by going to the Debug menu and in the drop down click Program
14. Push the Reset button on your board located near Port D

Verify: LED 4 is blinking and LED3 is “Breathing”.

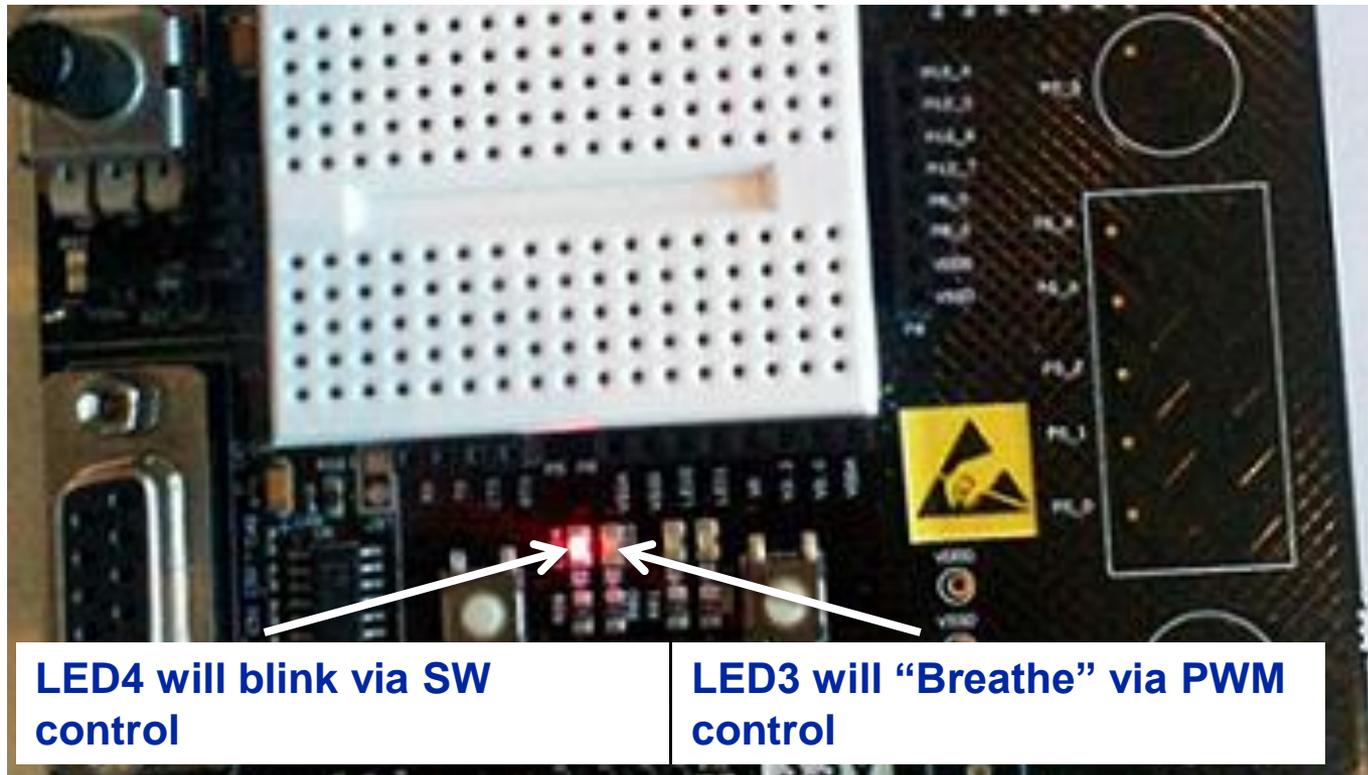
15. Re-program the board by going to the Debug and selecting Debug.
16. Start the program by clicking on the green arrow in the tool bar



17. Allow to run then halt execution-



Validate that LED4 has stopped blinking, LED3 continues to 'Breathe'. Why?



INTRODUCTION TO PSOC 3 AND PSOC 5LP

# ANALOG PERIPHERALS

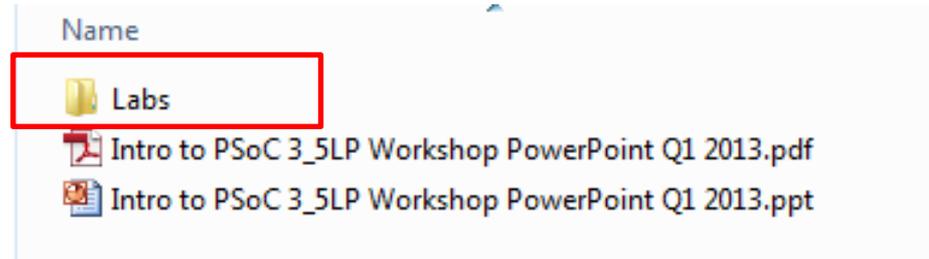
## LAB- LAB 2

## Lab Objective

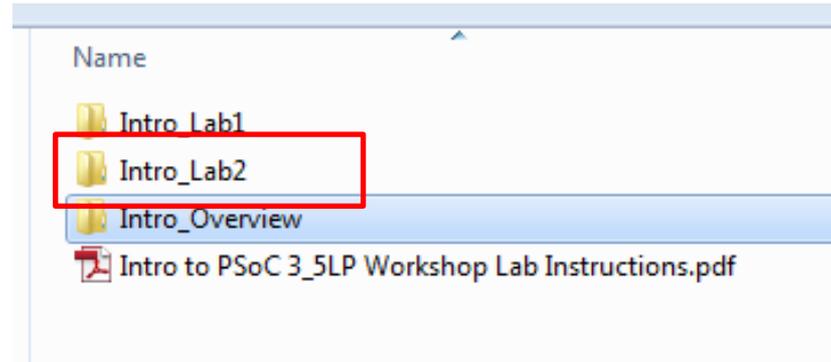
- To convert an output from the potentiometer into a digital number using the ADC
- To display the digital number on the LCD Screen on PSoC Development Kit

# Lab 2

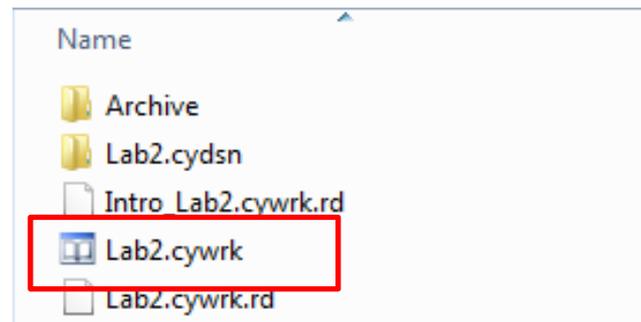
- Open Labs Directory



- Open Intro\_Lab2 Directory



- Double Click 'Lab2.cywrk'



## Instructions:

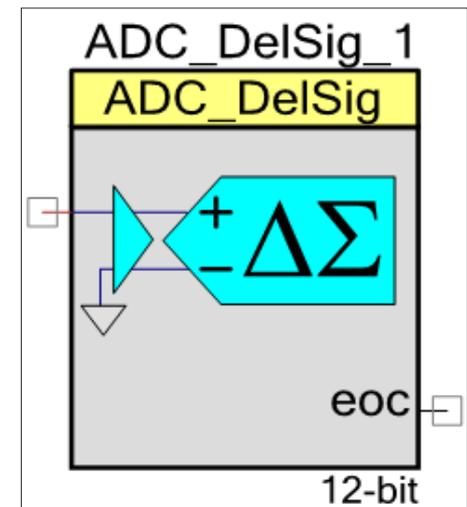
1. Place the Analog Pin from Component Catalog as shown here in the adjacent box



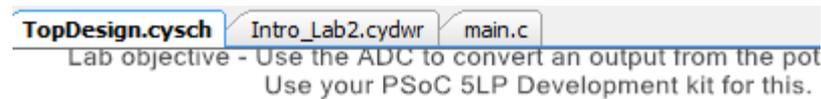
2. Place the Delta Sigma ADC in the box as shown below.
3. Double-click on the component to open it in the configuration mode and make the following changes:

### Set Properties to:

Conversion Mode: 1-Multi Sample	Input Mode: Single
Resolution: 12-Bits	Input Range: Vssa to Vdda
Conversion Rate: 1000 SPS	Buffer Gain: 1
Clock Frequency: 131 kHz (Calculated value)	Buffer Mode: Rail to Rail



4. Use the wire tool found on the left side of the worksheet (shown in slide 23) to connect Pin 1 to the ADC input. To use the wire tool hover over the connections until an 'X' appears, then click to make the connection.
5. Your final schematic should look like this when complete



1. Place Analog Pin Here
2. Place Delta Sigma ADC Here

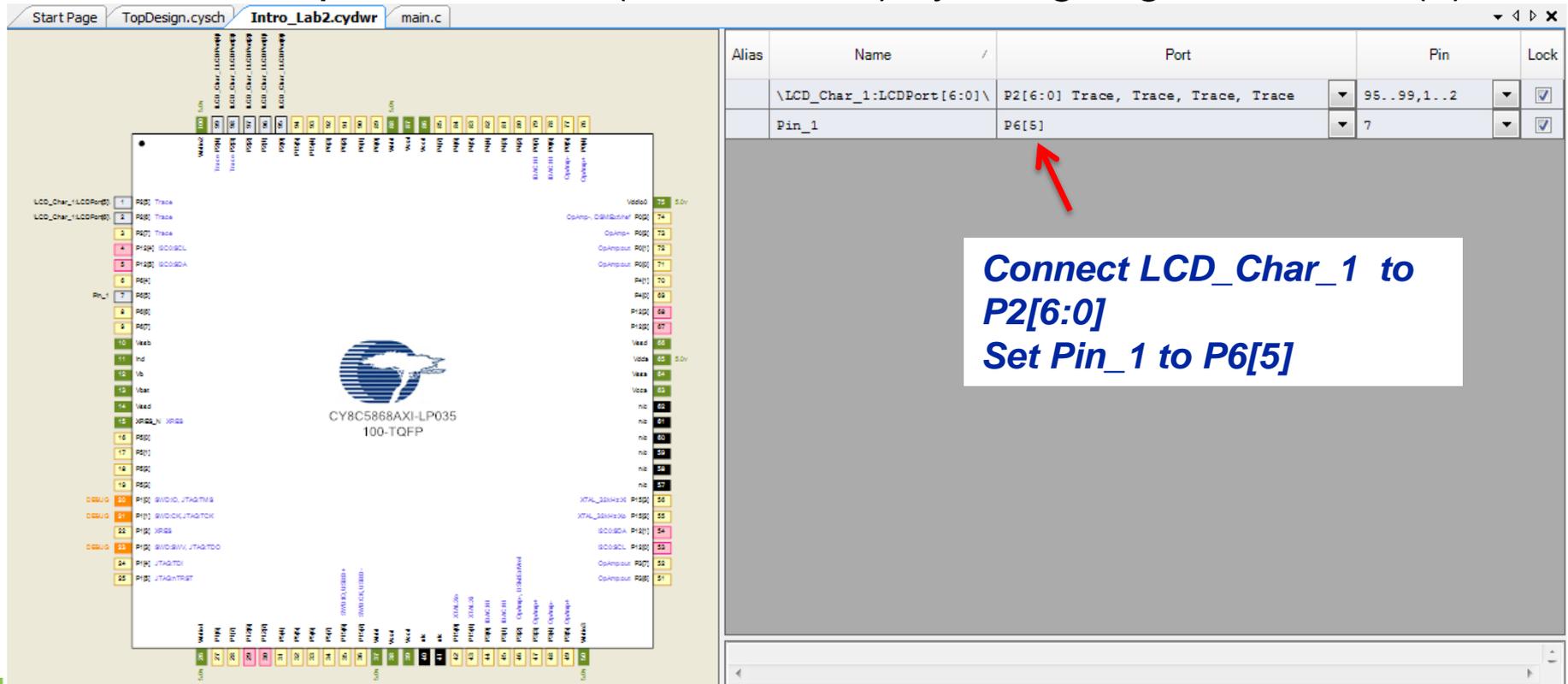


Set Properties to:

- Conversion Mode: 1-Multi Sample
- Resolution: 12-Bits
- Conversion Rate: 1000 SPS
- Clock Frequency: 131 kHz  
(Calculated value)
- Input Mode: Single
- Input Range: Vssa to Vdda
- Buffer Gain: 1
- Buffer Mode: Rail to Rail

# Lab 2

6. In the Workspace Explorer double click on the .cydwr file to open Design wide Resources (as explained in Overview lab)
7. In the Design wide Resources tab locate the section for pins on the right
8. Connect the LCD to Port 2 by assigning LCDPort[6:0] to P2[6:0]. Connect Pin 1 to the potentiometer (Port 6, Pin 5) by assigning Pin\_1 to P6(5).



The screenshot shows the Cypress IDE workspace with the 'Intro\_Lab2.cydwr' file open. The pin configuration table is visible on the right side of the workspace. A red arrow points to the 'Pin\_1' row in the table. A callout box with blue text provides instructions on how to connect the LCD and the potentiometer.

Alias	Name	Port	Pin	Lock
	\LCD_Char_1:LCDPort[6:0]\	P2[6:0] Trace, Trace, Trace, Trace	95..99,1..2	<input checked="" type="checkbox"/>
Pin_1		P6[5]	7	<input checked="" type="checkbox"/>

**Connect LCD\_Char\_1 to P2[6:0]  
Set Pin\_1 to P6[5]**

9. Build the project by going to the Build menu selecting Build System Resources Lab. This will take some time to build the project.
10. At this point, verify that the board is plugged in.
11. Program the board by going to the Debug menu and in the drop down click Program
12. Push the Reset button on your board located near Port D
13. Verify: When you turn the POT you should see the ADC values change

# Lab 2

