Introduction to PSoC®

Designing with PSoC 3 and PSoC 5LP using PSoC Creator 2.2

Q1 2013
Cypress Semiconductor Corp.

Before we begin

Install PSoC Creator 2.2 (if you haven't already)

- *Copy* PSoCCreatorSetup_2.2.exe *from the USB drive onto your desktop*
- Launch PSoCCreatorSetup_2.2.exe
- Follow installation prompts (typical)
- Raise hands for issues / questions

Copy the following Folder from the USB-drive to your desktop

- Intro to PSoC3_5LP Workshop Q1 2013
- Don't Place it too Deep in your Directory Tree

Verify you have the required hardware

- *PSoC 5 LP Kit (CY8CKIT-050)*

PSoC Development Kit

CY8CKIT-050 PSoC 5 LP

Agenda

Time	Topic
9:00 – 9:15 am	Setup and Install
9:15 – 9:45 am	PSoC 3, PSoC 5LP Architecture Overview
9:45 – 10:00 am	Architecture Overview Lab
10:00 – 10:15 am	System Resources
10:15 – 10:30 am	BREAK
10:30 – 10:45 am	Digital Peripherals
10:45 – 11:15 am	Digital Peripherals – Lab 1
11:15 – 11:30 pm	Analog Peripherals
11:30 – 12:00 pm	Analog Peripherals – Lab 2
12:00 – 12:30 pm	BREAK

INTRODUCTION TO PSOC 3 AND PSOC 5LP

ARCHITECTURE OVERVIEW

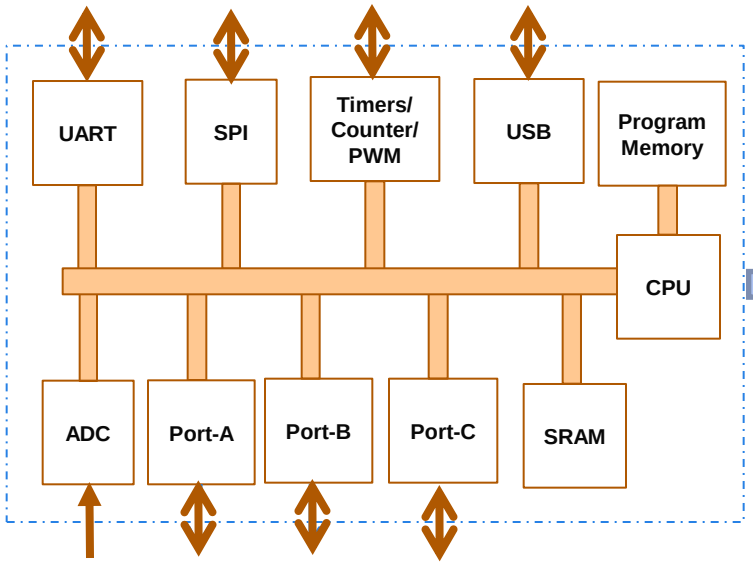
Section Objectives

At the end of this section you will be able to

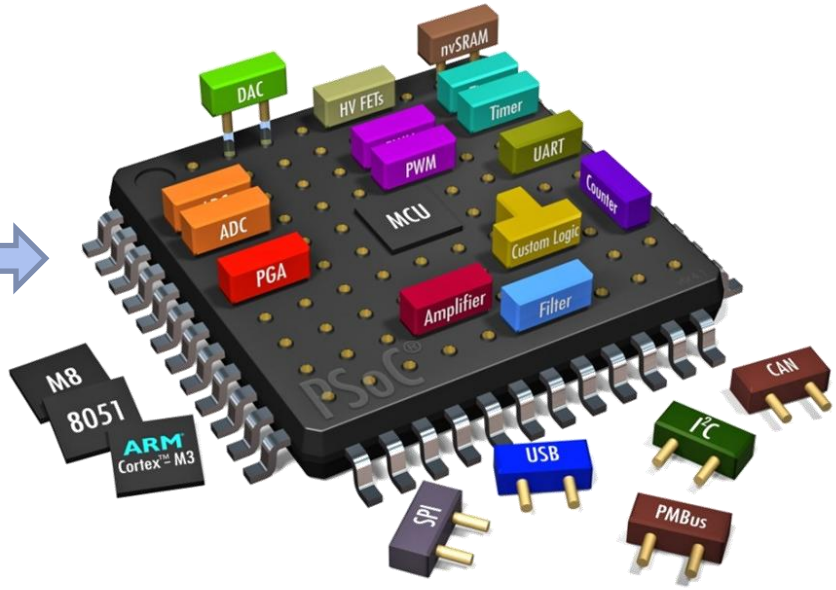
- Understand the high-level architecture of PSoC 3 and PSoC 5LP
- Understand the CPU, Digital, Analog and Programmable Routing / Interconnect Systems

PSoC – The Future of Embedded Design

Traditional MCU architecture



PSoC – The future of embedded architecture



PSoC is the world's only Programmable System on Chip integrating programmable analog and digital functions, flexible routing and interconnect, memory and a microcontroller on a single chip.

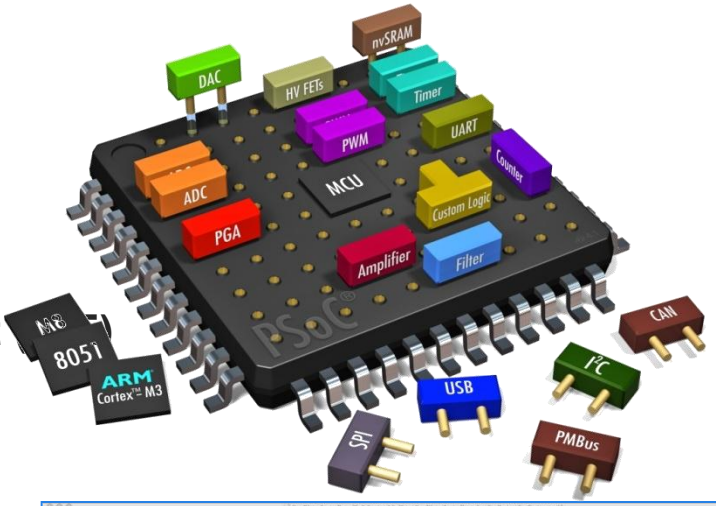
Programmable System on Chip

PSoC is a programmable system on a single chip

Microcontroller is a sub system of PSoC

Programmable high-precision analog and digital

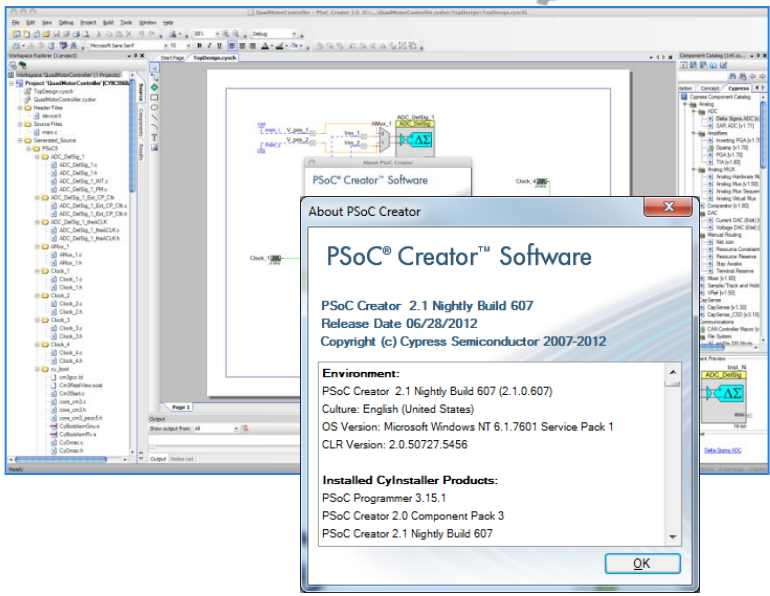
Flexible routing and interconnect



PSoC Creator™ integrated development environment

80+ production-ready mixed signal Components

Includes the GNU C/C++ compiler and GDB debugger



Leverages ARM ecosystem

Seamless export/debug support

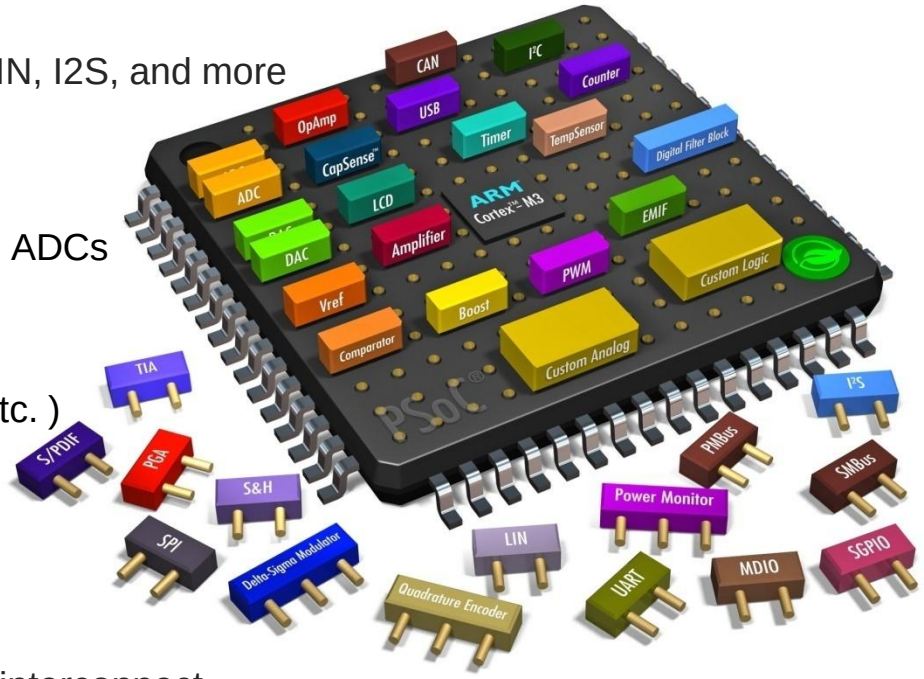
PSoC 5LP addresses the need of precision analog integration on a flexible, low power ARM based system on a single chip.

The combination of PSoC 5LP and Creator software allows for innovation and differentiation with shorter development schedules

PSoC 5LP - Precision Analog 32-bit PSoC

32-bit ARM Cortex-M3 based MCU

Runs up to 67MHz (80MHz in 2H13), 1.25 DMIPS/MHz CPU performance, 1KB Cache
Up to 256KB of Flash, 64KB of SRAM
Communication interfaces: CAN, USB, I2C, SPI, UART, LIN, I2S, and more



Unmatched precision analog integration

Best-in-class accurate & precise 12-bit SAR, 20-bit DelSig ADCs
Precision Analog Components
- OpAmps, Comparators, 8-bit I/VDAC, CapSense, LCD
- Programmable Analog Blocks (TIA, S&H, PGA, Mixer, etc.)

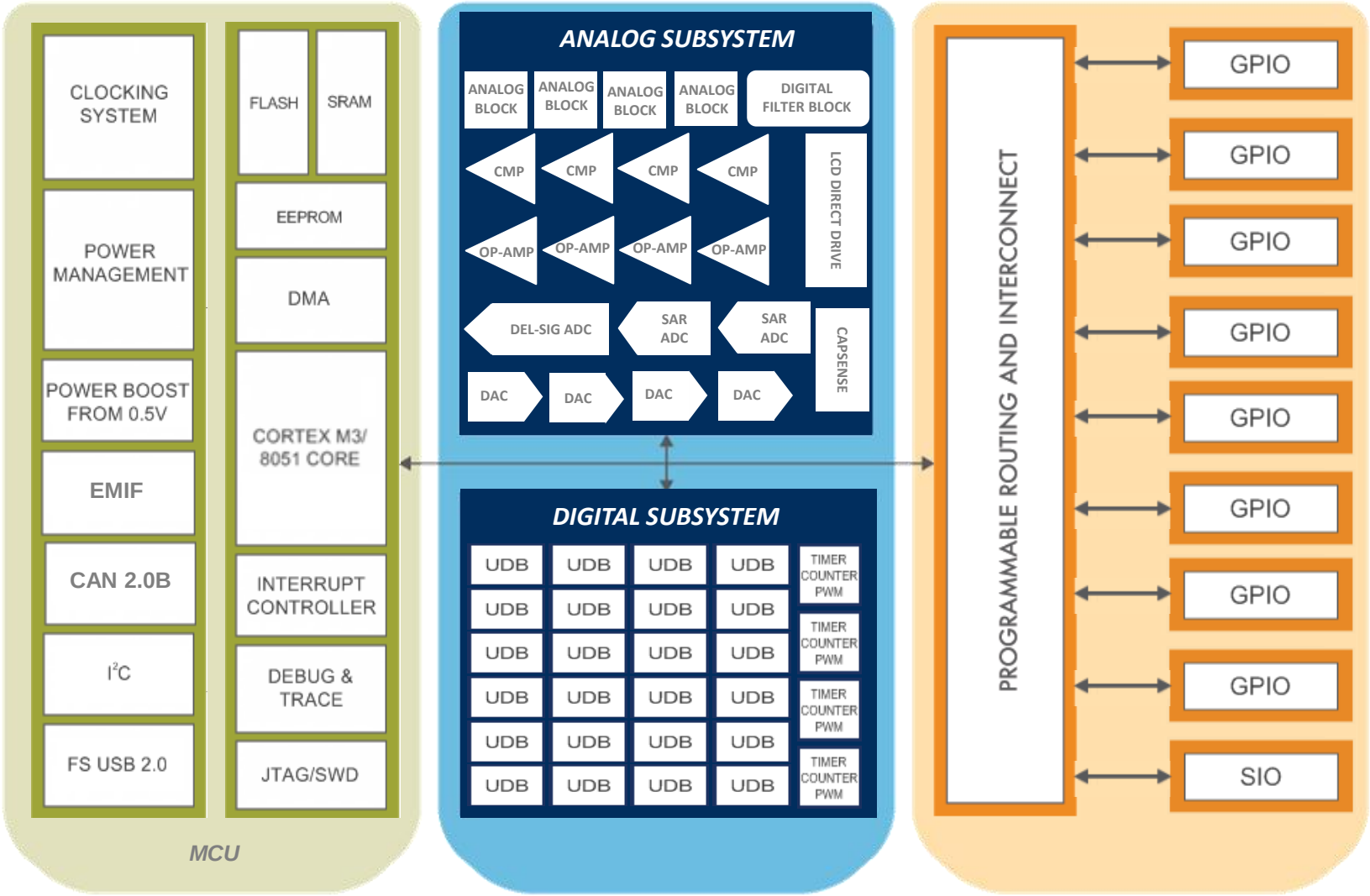
1.024V ±0.1% on-chip reference voltage
Fully functional analog from 1.71V to 5.5V

The most flexible low power PSoC

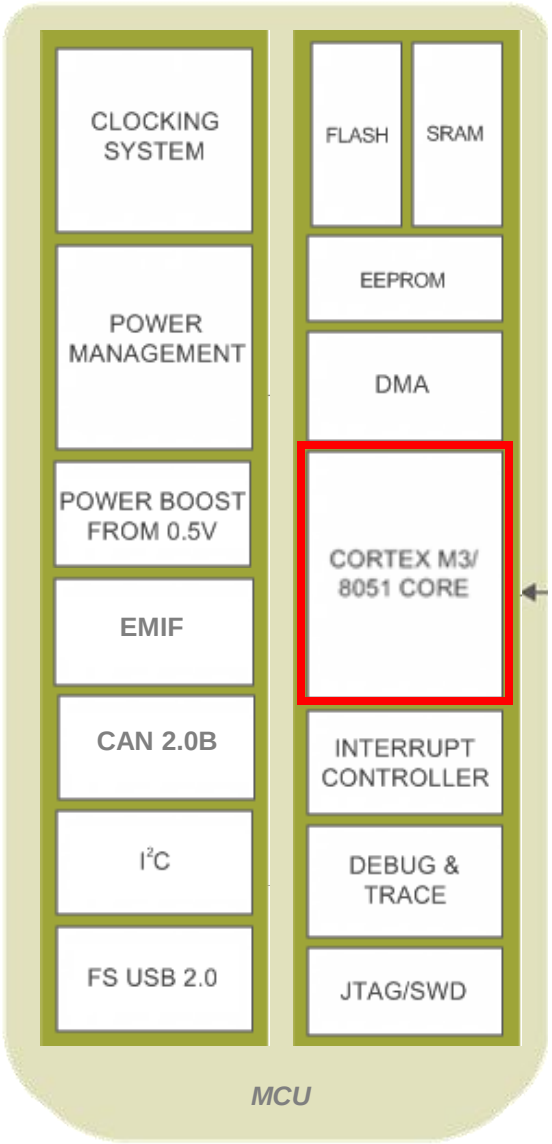
Programmable analog and digital with flexible routing and interconnect
Device startup with Boost from 0.5V
Industry's widest device operating range 0.5V to 5.5V
Lowest power consumption
Consuming **300 nA** in hibernate mode while retaining CPU, SRAM, device configuration, can wake up on IOs

The most flexible low power system on chip with precision analog and easy to use software

PSoC 3 / PSoC 5LP Platform Architecture



MCU Subsystem



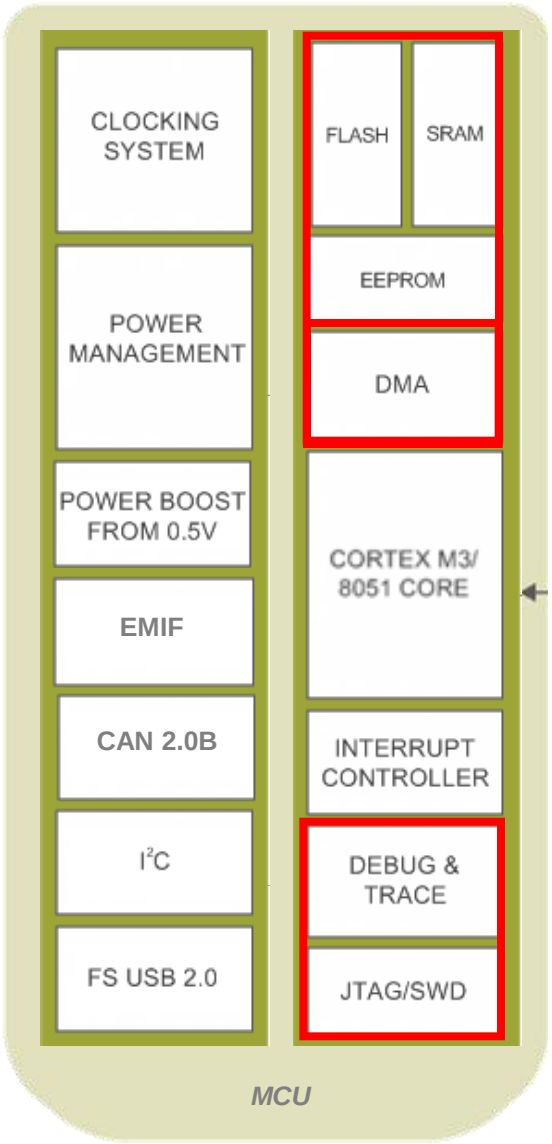
ARM Cortex-M3

- Low power, low interrupt latency, 32-bit CPU
- Broad support for middleware and applications
- Up to 67 MHz; 83 DMIPS; 1KB Cache Memory
- Enhanced v7 ARM architecture
- Thumb2 Instruction Set
- 16- and 32-bit Instructions - no mode switching req.
- 32-bit ALU; Hardware single-cycle multiply&divide
- Single cycle 3-stage pipeline; Harvard architecture

8051

- Low power, 8-bit CPU
- Broad base of existing code and support
- Up to 67 MHz; 33 MIPS
- Single cycle instruction set

MCU Subsystem



High Performance Memory

- 256KB Code and 32KB Flash Memory with ECC
- High ratio of SRAM to flash; 64KB SRAM
- 2KB EEPROM
- External Memory Interface up to 16MB (EMIF)

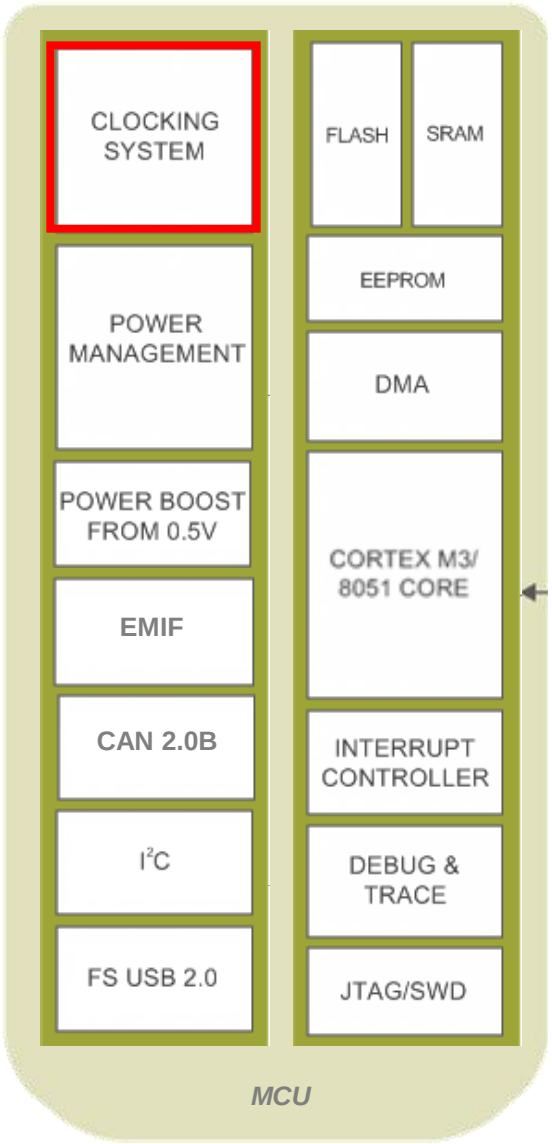
Powerful DMA Engine

- 24-Channel Direct Memory Access
- Access to all Digital and Analog Peripherals
- CPU and DMA simultaneous access to independent SRAM blocks

On-Chip Debug and Trace

- Industry standard 2-wire SWD, 4/5-wire JTAG
- On-chip 4bit data width TRACE, SWV

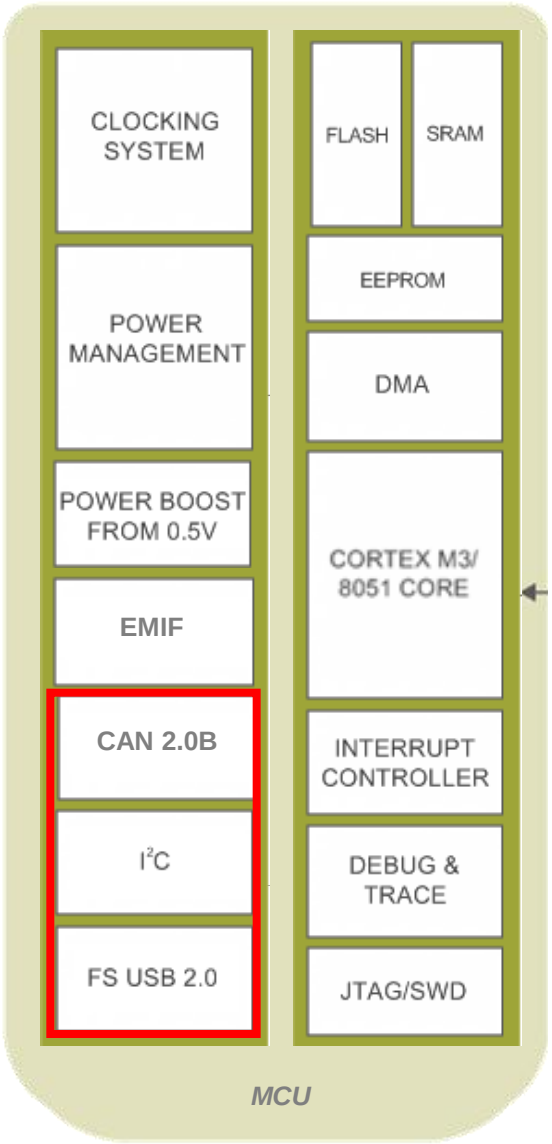
MCU Subsystem



Clocking System

- Multiple Clock Sources
  - Crystal-less Internal Main Oscillator
  - External MHz crystal input
  - External clock inputs
  - Clock doubler output
  - Internal low speed oscillator
  - External 32 kHz crystal input
  - Dedicated 48 MHz USB clock
  - PLL output
- 16-bit Clock Dividers
  - 8 Digital Domain
  - 4 Analog Domain
- PSoC Creator Configuration Wizard
- PSoC Creator auto-derives clocking sources / dividers

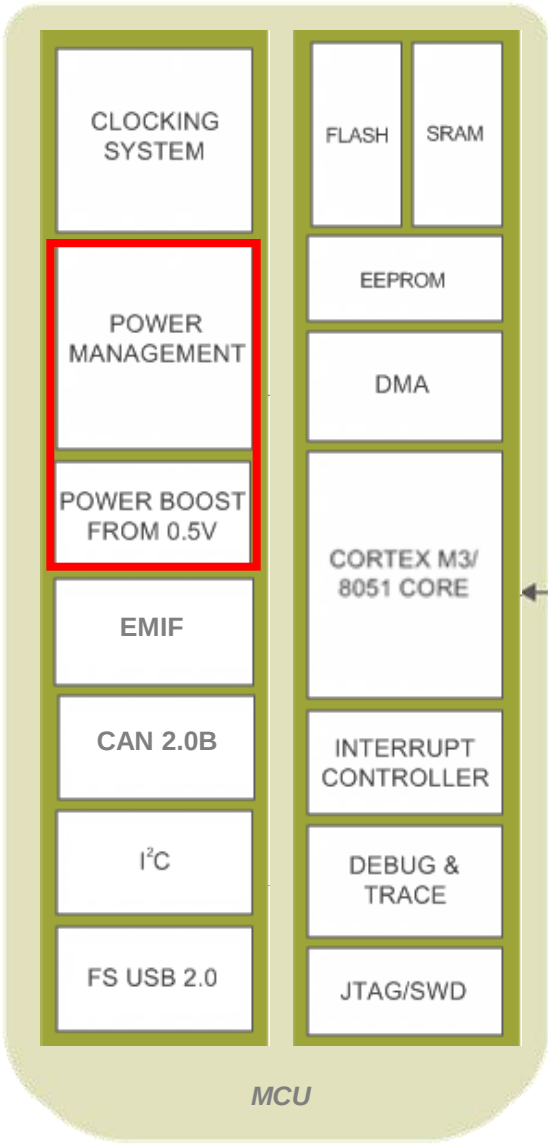
MCU Subsystem



Dedicated Communication Peripherals

- Full Speed USB Device
  - 8 bi-directional data end points + 1 control end point
  - No external crystal required
  - Drivers in PSoC Creator for HID class devices
- Full CAN 2.0B
  - 16 RX buffers and 8 TX buffers
- I2C master or slave
  - Data rate up to 400 kbps
  - Additional I2C slaves may be implemented in UDB array
  - Multi-Master mode supported

MCU Subsystem



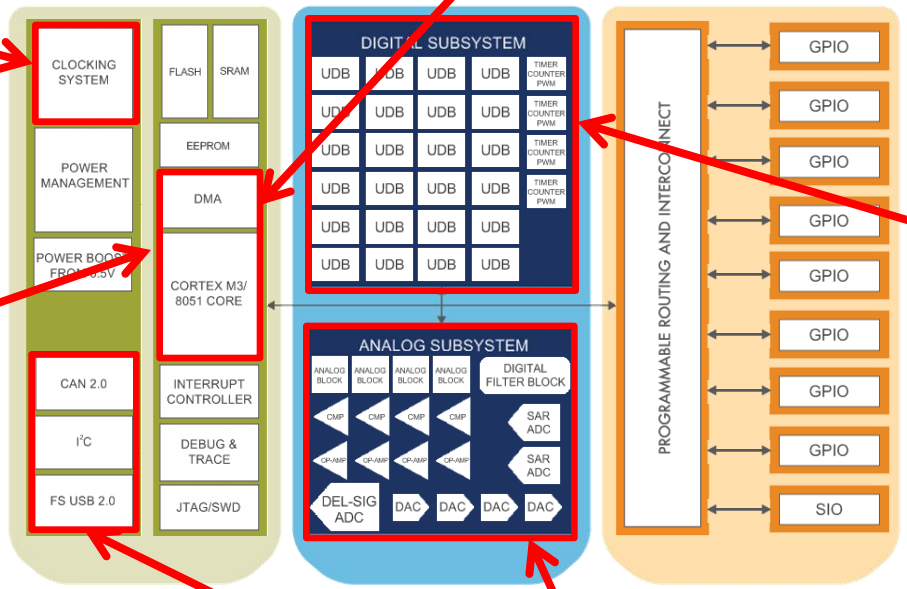
Power Management

- Industry's Widest Operating Range
  - 0.5V to 5.5V with Boost
- The only Single-Cell Battery operated ARM embedded processor – PSoC 5LP
- High Performance at 0.5V
  - PSoC 3 and PSoC 5LP @ 67 MHz
- 4 Power Modes (Active, Alternate Active, Sleep and Hibernate)
  - Easy to use APIs in Creator software for Power Management

Designed for Low Power / Low Voltage

On-board DMA Controller
Direct Memory transfer between peripherals offloads CPU operation, lowering power consumption

Highly configurable clock tree
Most flexible, automated clock



Universal Digital Blocks
Implement features in hardware that reduce CPU processing requirements, lowering power consumption

Cached Operations
Execution from flash memory is improved by caching instructions (PSoC 5 only)

Precise CPU Frequencies
PLL allows 4032 different frequencies, tunable power consumption

Integrated Analog, Digital and Communications Peripherals
Reduce external component counts and lower overall **system** power consumption

Low Power Modes

PSoC 3
8051

Power Mode	Current	Code Execution	Digital Resources Available	Analog Resources Available	Clock resources Available	Wakeup Sources	Reset Sources
Active	1.2 mA @ 6 MHz	Yes	All	All	All	N/A	All
Sleep	1 uA	No	I2C	Comparator (CMP)	ILO/ 32kHz ECO	CMP, PICU, I2C, RTC, CTW, LVD	XRES, LVD, WDR
Hibernate	200 nA	No	None	None	None	PICU	XRES, LVD

PSoC 5LP
ARM
Cortex-M3

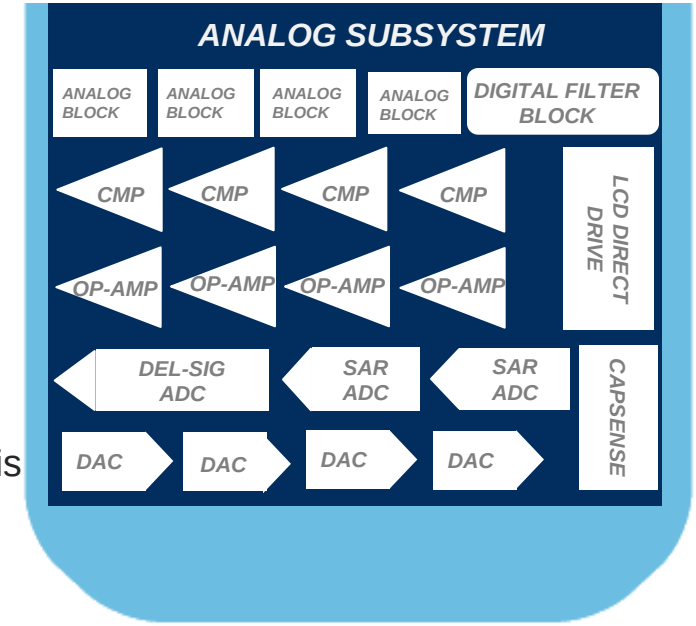
Power Mode	Current	Code Execution	Digital Resources Available	Analog Resources Available	Clock resources Available	Wakeup Sources	Reset Sources
Active	3.1 mA @ 6 MHz	Yes	All	All	All	N/A	All
Sleep	2 uA	No	None	Comparator (CMP)	ILO/ 32kHz ECO	CMP, PICU, I2C, RTC, CTW, LVD	XRES, LVD, WDR
Hibernate	300 nA	No	None	None	None	PICU	XRES, LVD

ILO – Internal Low Speed Oscillator
ECO – External Crystal Oscillator
CMP - Comparator
PICU – Port Interrupt Control Unit
RTC – Real Time Clock
CTW – Central Time Wheel
LVD – Low Voltage Detect
XRES – External Reset
WDR – WatchDog Reset

Programmable Analog Subsystem

Programmable Precision Analog

- **Flexible Routing:** All GPIO are Analog I/O
- **Precision analog**
  - 8 to 20-bit Delta-Sigma ADC
  - Two 1Msps 12-bit SAR ADCs
  - 1.024V ±0.1% accurate on-chip reference voltage
- **4x Comparators**
  - 4mV Input Offset, 75ns response time, Max 32mV Hysteresis
  - Ultra low power mode with CPU wakeup capability
- **4x OpAmps**
  - 2mV Input Offset, 3MHz Bandwidth, 25 mA drive capability
- **4x VDACs / IDACs**
  - 1Msps ±2.5 LSB INL VDAC or 8Msps ±1 LSB INL IDAC;
  - 8-bit resolution, ±1 LSB DNL
- **Analog Mux**
  - Up to 62 inputs; routing from any pin to all analog Components
- **4x SC/CT(switch capacitor/continuous time) blocks**
  - Configurable to PGA, TIA, Mixer, Sample & Hold, and other functions

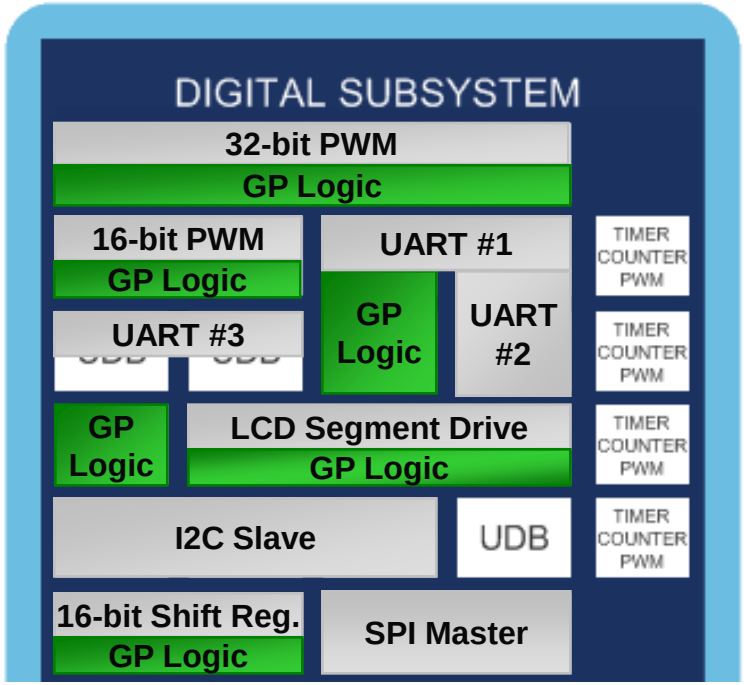


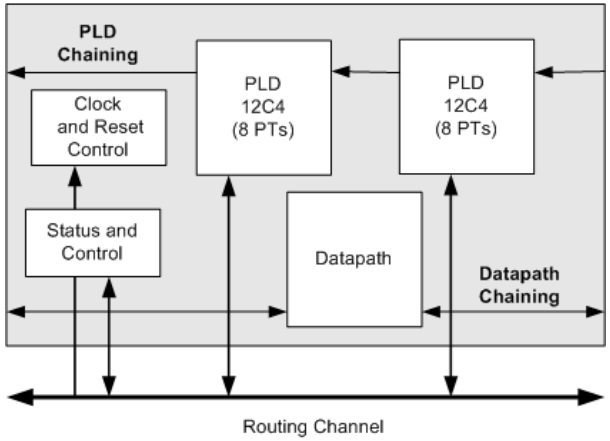
- **LCD direct drive**
  - up to 46x16 segments (736 Segments)
- **Capacitive touch sensing**
  - on all 62 GPIO pins
- **Digital Filter capability**
  - 24-bit filter co-processor
  - up to 4 HW IIR & FIR filters
  - Two separate filter channels
  - Four cascaded filters per channel

Programmable Digital Subsystem

UDB - Universal Digital Block

- Programmable logic-based digital system comprised of 24 UDBs
- Each UDB consists of:
  - 8 Macro Cells
  - 8-bit Datapath and Registers
  - Flexible Interconnect
  - 24 Inputs, 8 Outputs
- Flexible Routing allows any GPIO to digital I/O
- Build custom logic functions and non-standard interfaces
- Build unique and differentiated functions like S/PDIF, PRS, SGPIO controller, and more
- Offload traditional CPU functions to hardware state machine, LUT, math functions
- Build functions with Cypress supplied primitives or even write your own Verilog Components in Creator

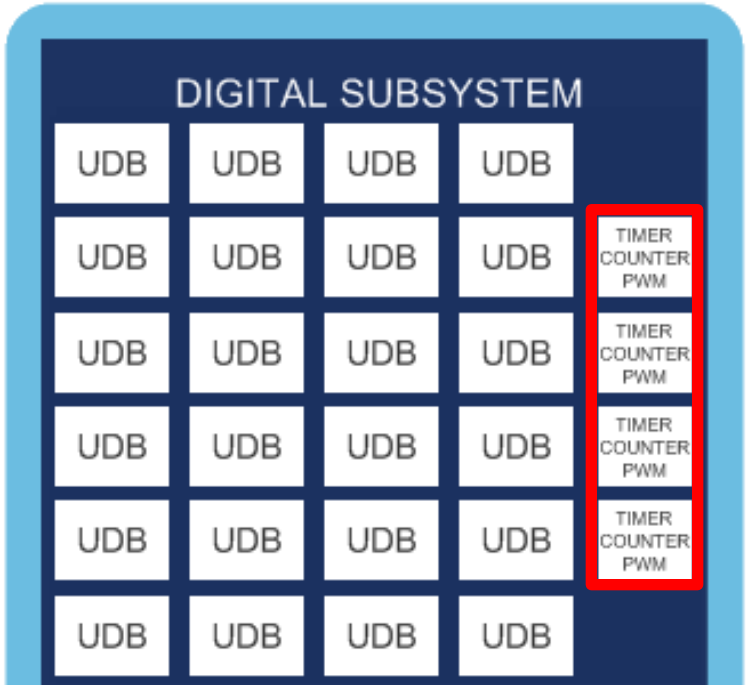




Programmable Digital Subsystem

Organized 16-bit Timer/Counter/PWM Blocks

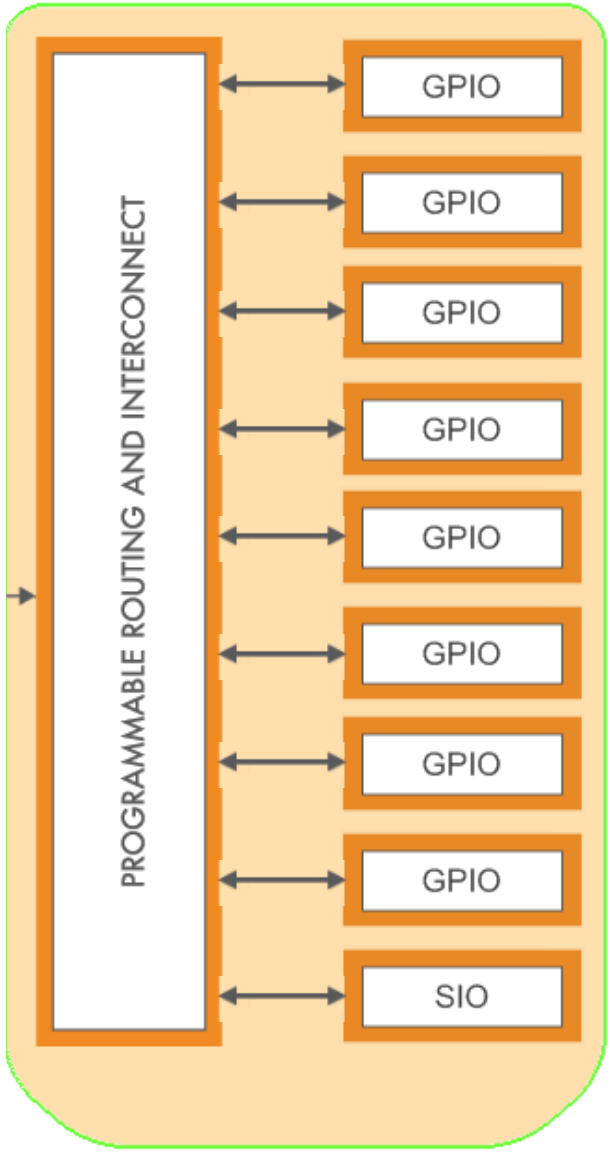
- Provides nearly all of the features of a UDB based timer, counter or PWM
- PSoC Creator provides easy access to these flexible blocks
- Each block may be configured as either a full featured 16-bitTimer, Counter or PWM. Two blocks may be combined to make it 32-bit
- Programmable options
  - Clock, enable, reset, capture, kill from any pin or digital signal on chip
  - Independent control of terminal count, interrupt, compare, reset, enable, capture and kill synchronization
- Plus
  - Configurable to measure pulse-widths or periods
  - Buffered PWM with dead band and kill



Programmable Routing/Interconnect

Input / Output System

- Three types of I/O
  - GPIO, SIO, USBIO
- Any GPIO to any peripheral routing
- Wakeup from sleep on analog, digital or I2C events
- Programmable slew rate reduces power and noise
- Eight different configurable drive modes
- Programmable input threshold capability for SIO
- Automatic and custom/lock-able routing in PSoC Creator



Four separate I/O voltage domains

- Interface with multiple devices using one PSoC 3 / PSoC 5 device

Review

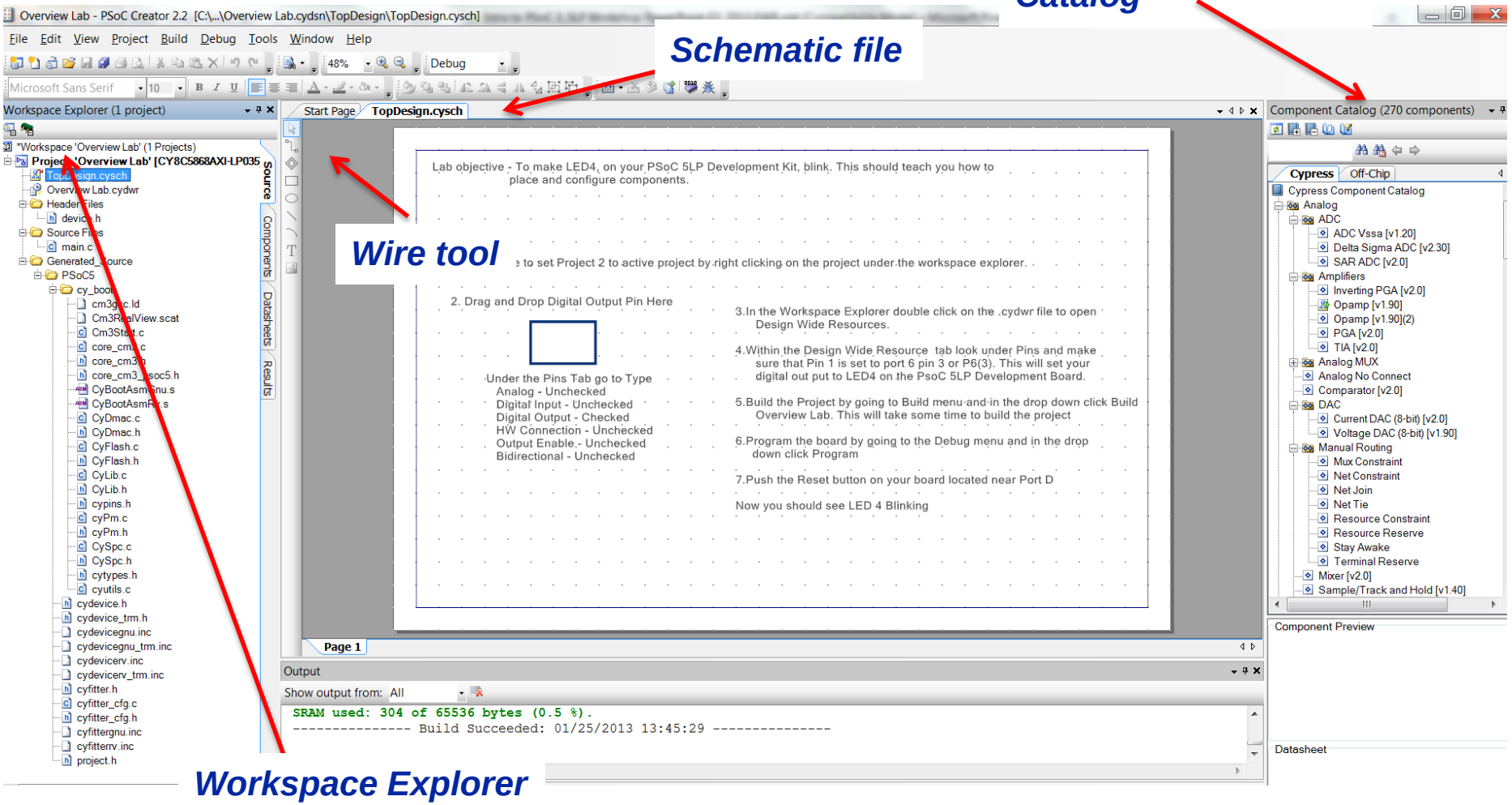
You should now be able to:

- Understand PSoC Architecture
- Understand the CPU, Analog, Digital and Programmable Routing and Interconnect Subsystems

INTRODUCTION TO PSOC 3 AND PSOC 5LP

ARCHITECTURE OVERVIEW LAB - WALKTHROUGH

PSoC Creator 2.2 Interface



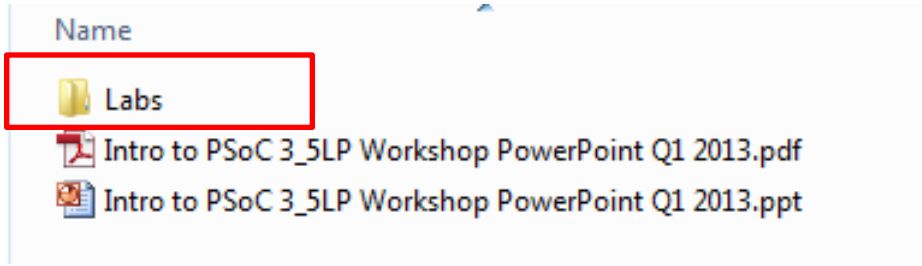
Architecture Overview Lab

Lab Objective

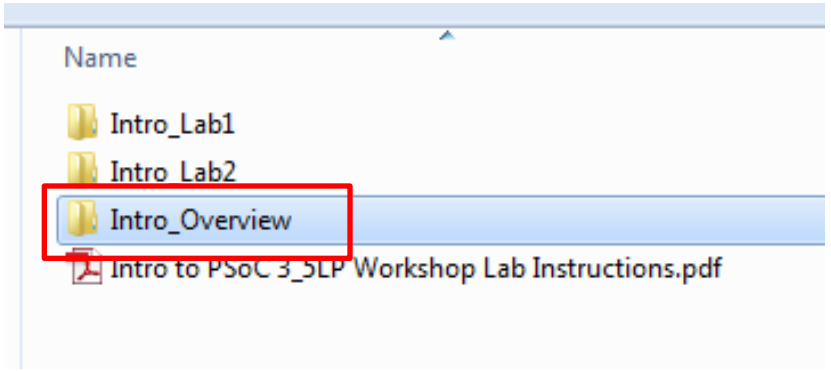
- To make LED4 on your PSoC Development Kit blink.
- To learn how to place and configure components in PSoC Creator

Architecture Overview Lab

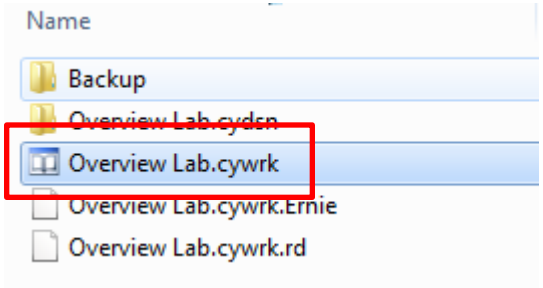
- Open Labs Directory



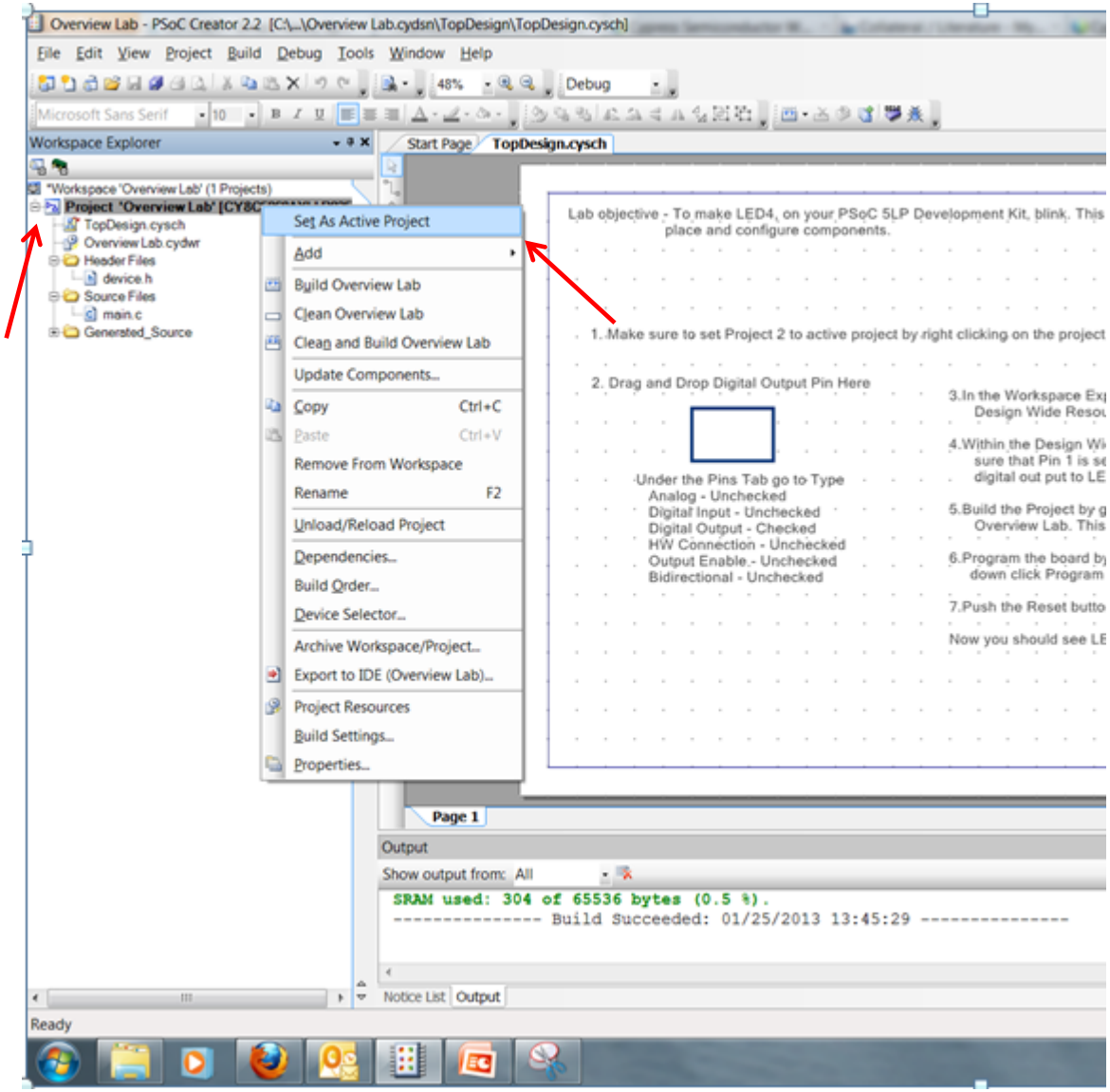
- Open Intro_Overview Directory



- Double Click 'Overview Lab.cywrk'



Architecture Overview Lab

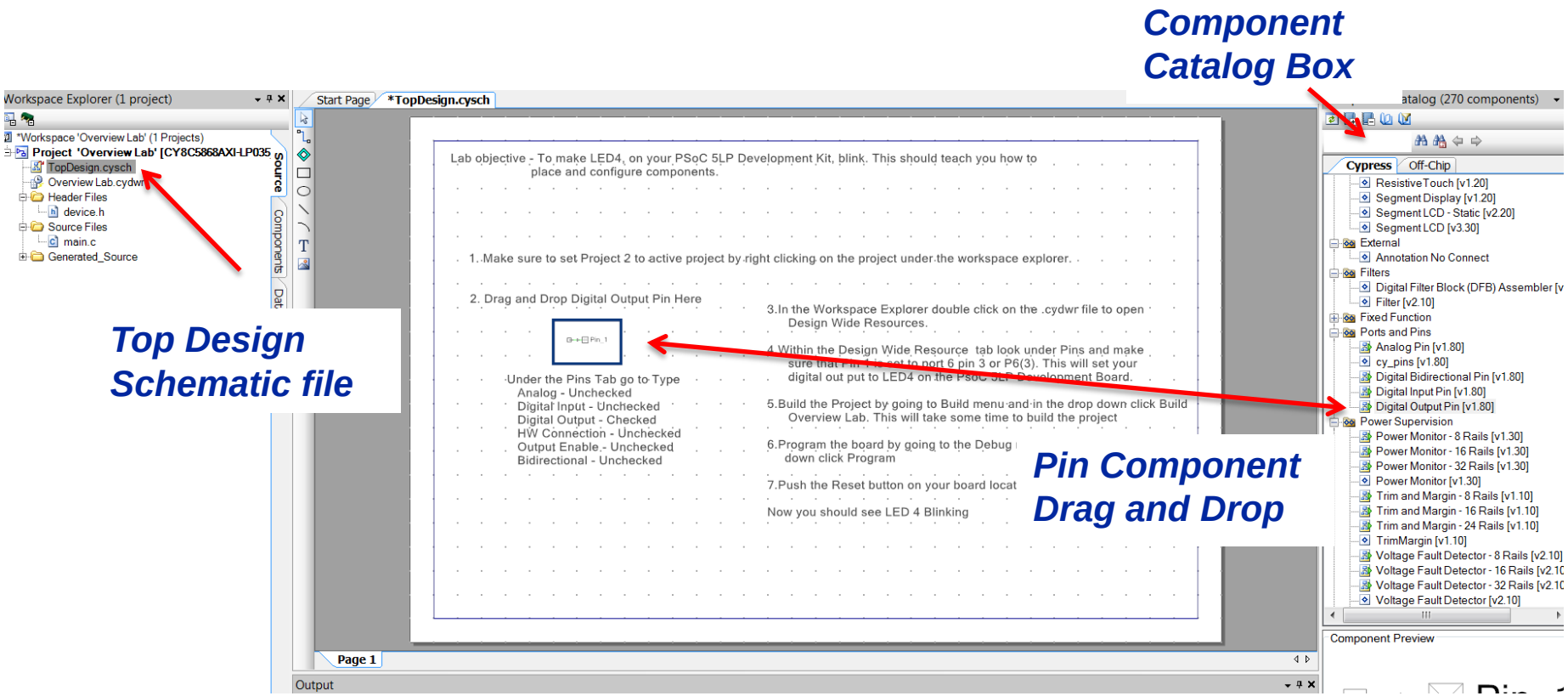


1. Set Project as active project by right clicking on the project under the workspace explorer as shown. Project will then be highlighted in Bold.

2. Then, expand the “+” sign to the left of Project to view project files. Double-click the schematic file “TopDesign.cysch” to open it

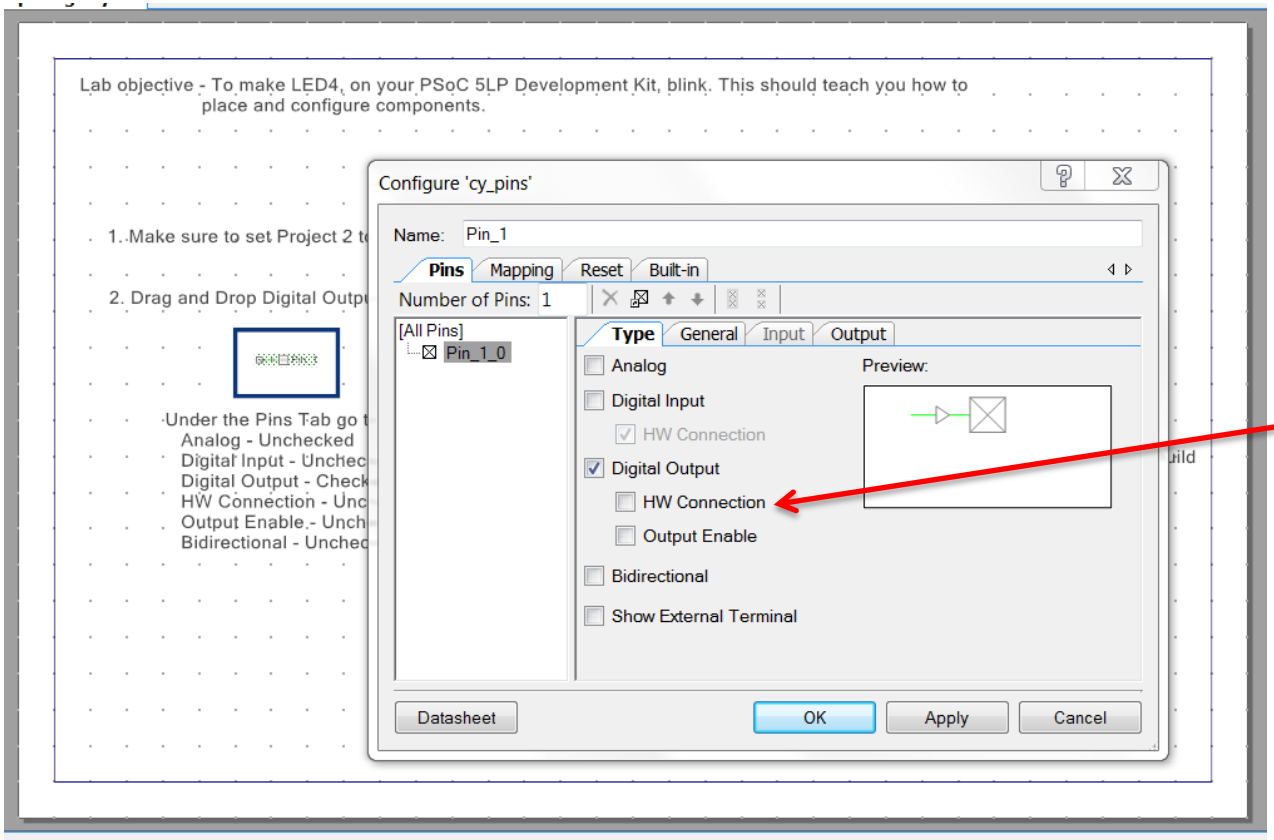
Architecture Overview Lab

3. From the “Component catalog” on the right side of the screen, drag & drop “Digital Output Pin” under “Ports and Pins” into the box (as shown below)



Architecture Overview Lab

4. Double-click the component to open it in configuration mode and check the configuration as follows:



Analog - Unchecked

Digital Input – Unchecked

Digital Output – Checked

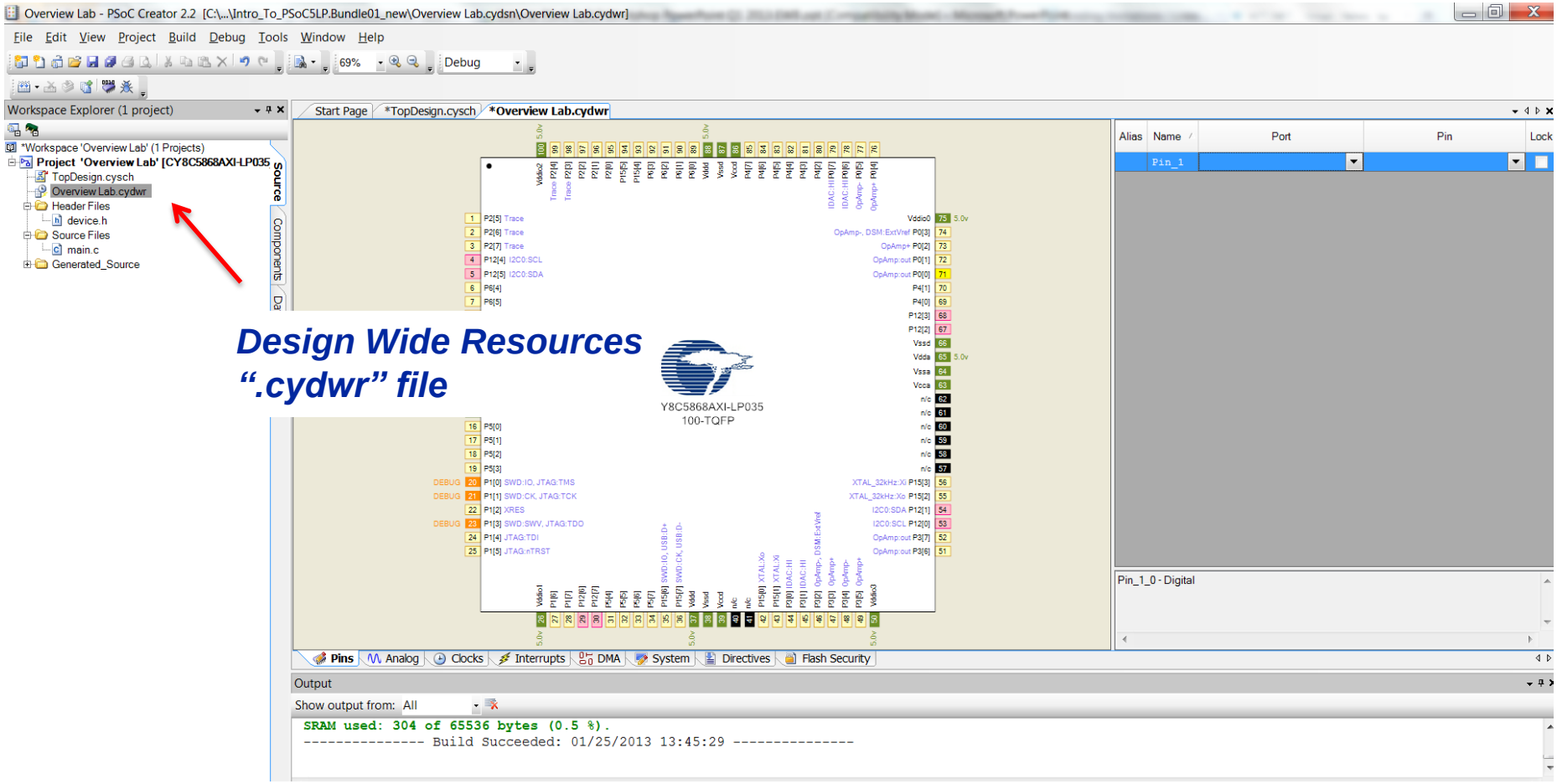
HW Connection – Unchecked

Output Enable – Unchecked

Bidirectional – Unchecked

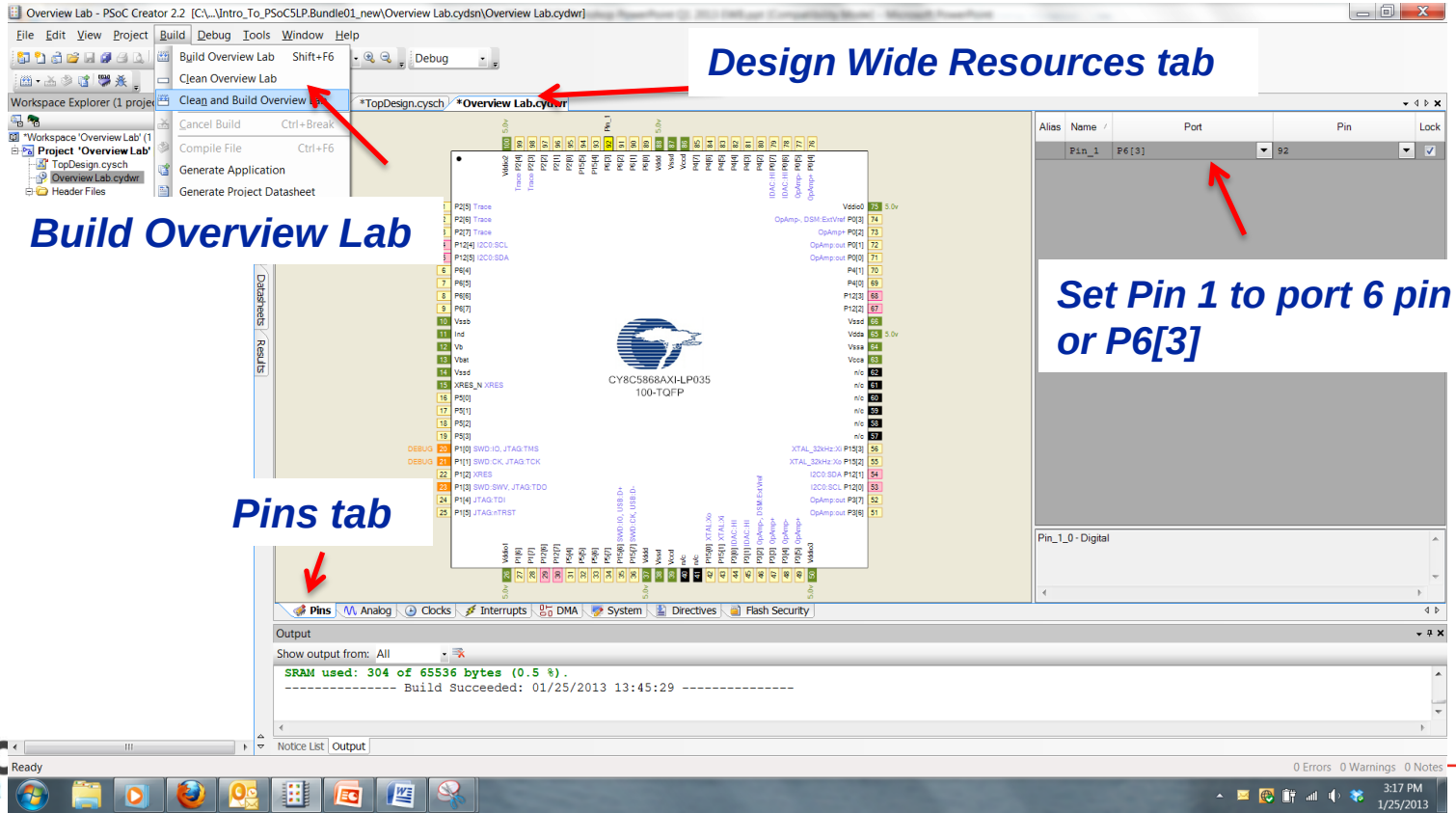
Architecture Overview Lab

5. In the Workspace Explorer double click on the .cydwr file to open Design Wide Resources



Architecture Overview Lab

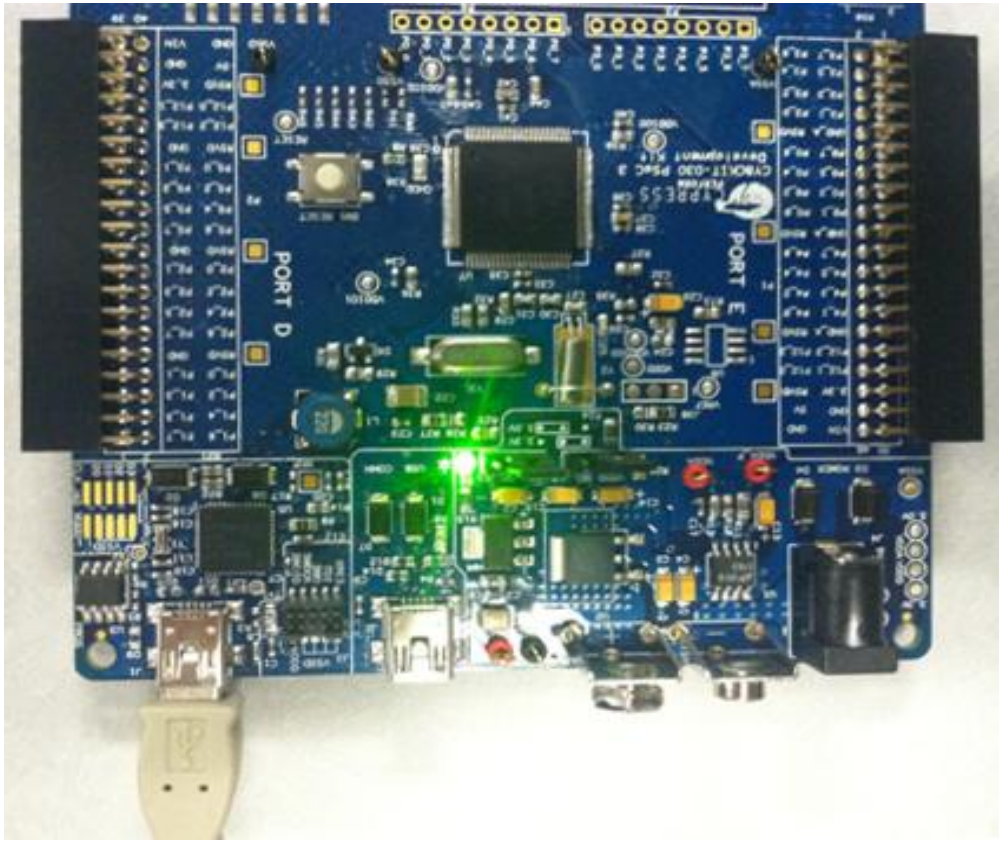
6. Within the Design Wide Resources tab, select the Pins tab (below the chip)
7. On the right hand side of the screen, make sure that Pin 1 is set to port 6 pin 3 or P6[3]. This will set your digital output to LED4 on the PSoC Development Board.
8. Build the Project by going to the Build menu and in the drop down click “Build Overview Lab”. This will take a minute to build the project.



Architecture Overview Lab

9. At this time, if you haven't already, plug in the USB cable from the kit (as shown in the picture below) into the board and plug in the other end into the computer.

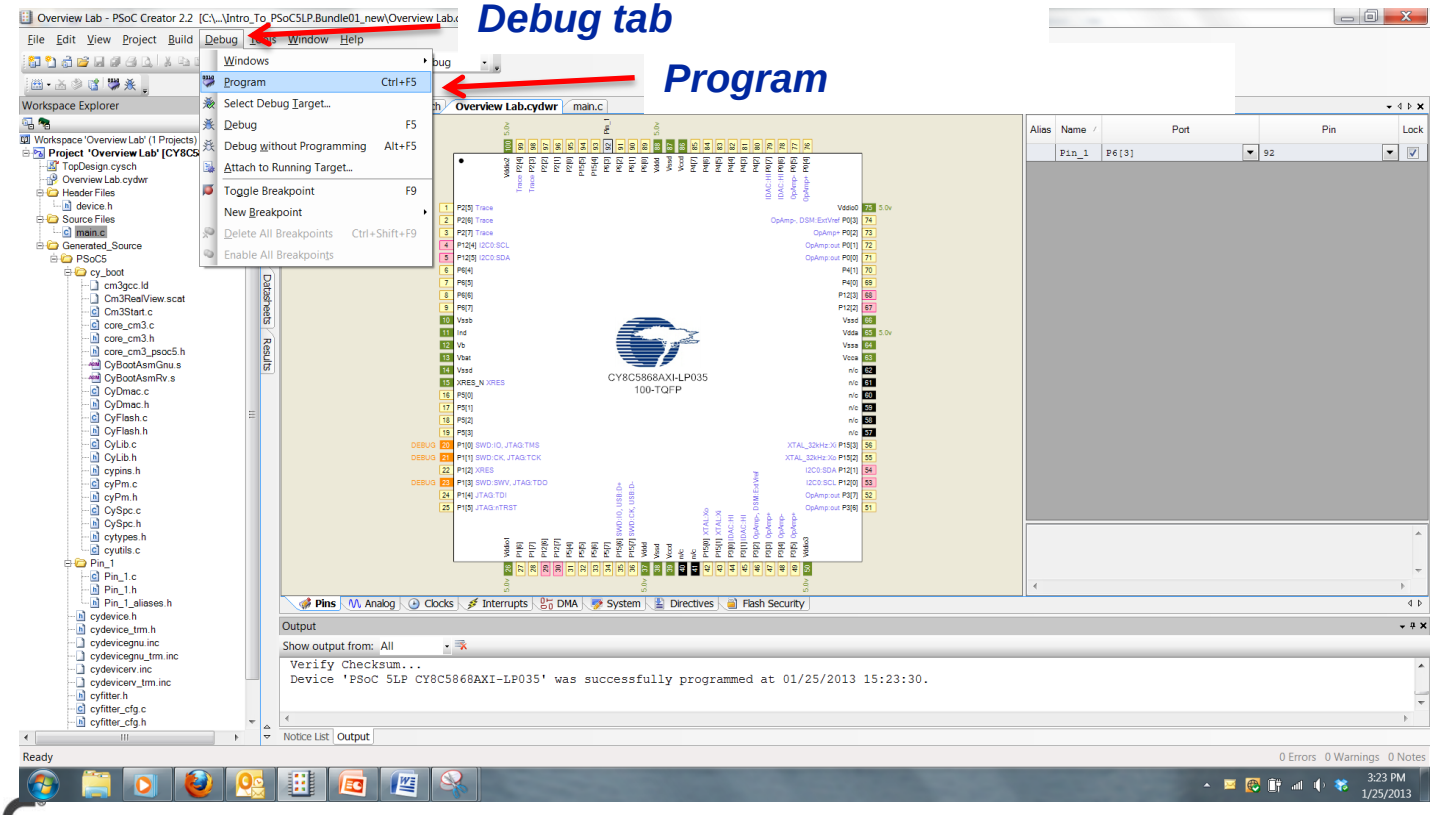
   If this is the first time that you are plugging in into the board, you may have to go through driver installation.



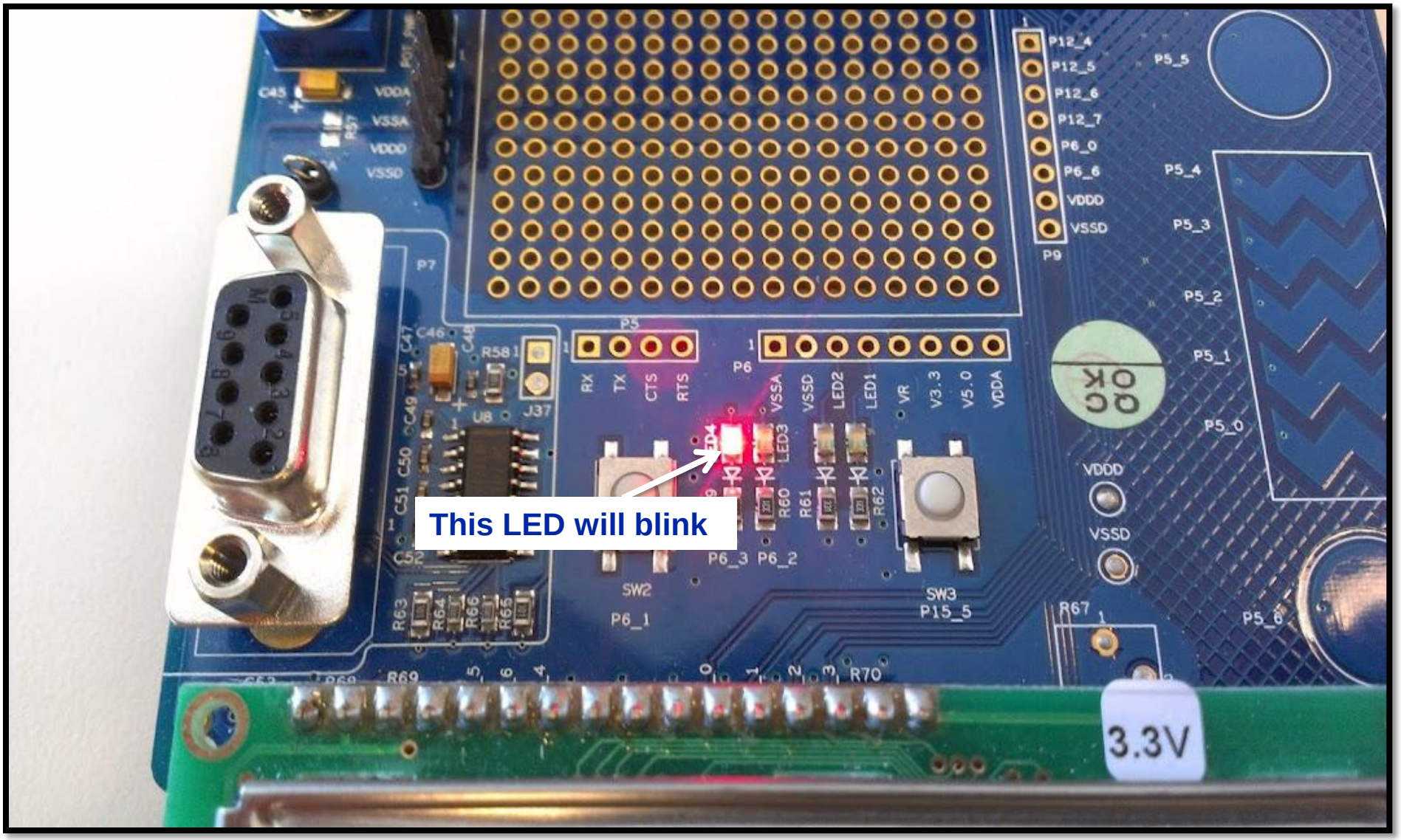
Architecture Overview Lab

10. Program the board by going to the Debug menu and click Program from the drop down list. Programming should take just a minute. You may have to select your kit and follow the steps to click on “Port Acquire”.
11. Push the Reset button on your board located near Port D

Verify that you see LED 4 Blinking.



Architecture Overview Lab



INTRODUCTION TO PSOC 3 AND PSOC 5LP

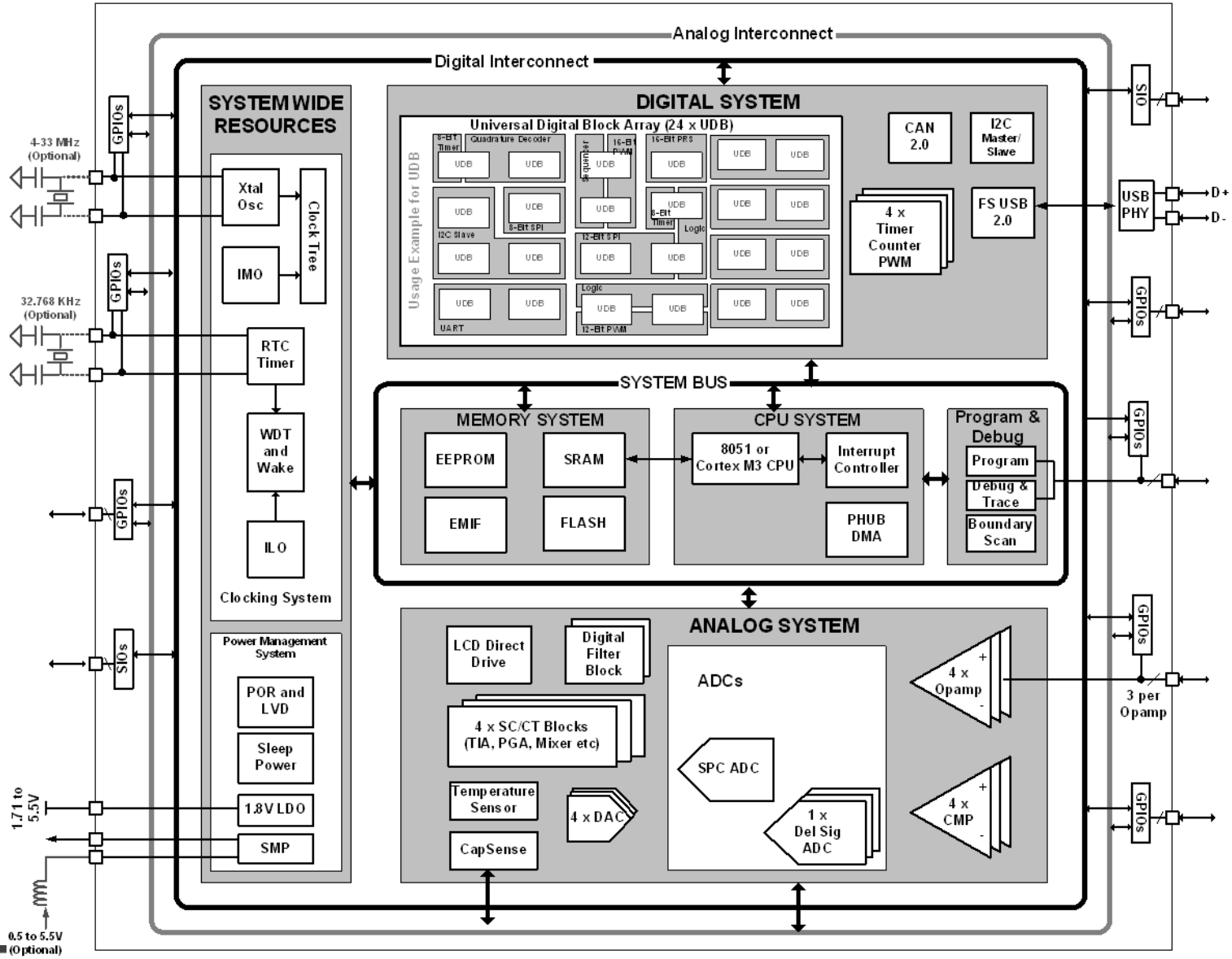
SYSTEM RESOURCES

Section Objectives

At the end of this section you will be able to

- Understand the system block diagram of PSoC 3 / PSoC 5LP devices
- Understand and use the PSoC 3 / PSoC 5LP System Resources, including:
  - Power System
  - Programming and debugging
  - Configuration and boot process
  - Resets
  - Clocking
  - Memory and Mapping
  - DMA and PHUB
  - I/O
  - Interrupts

System Block Diagram



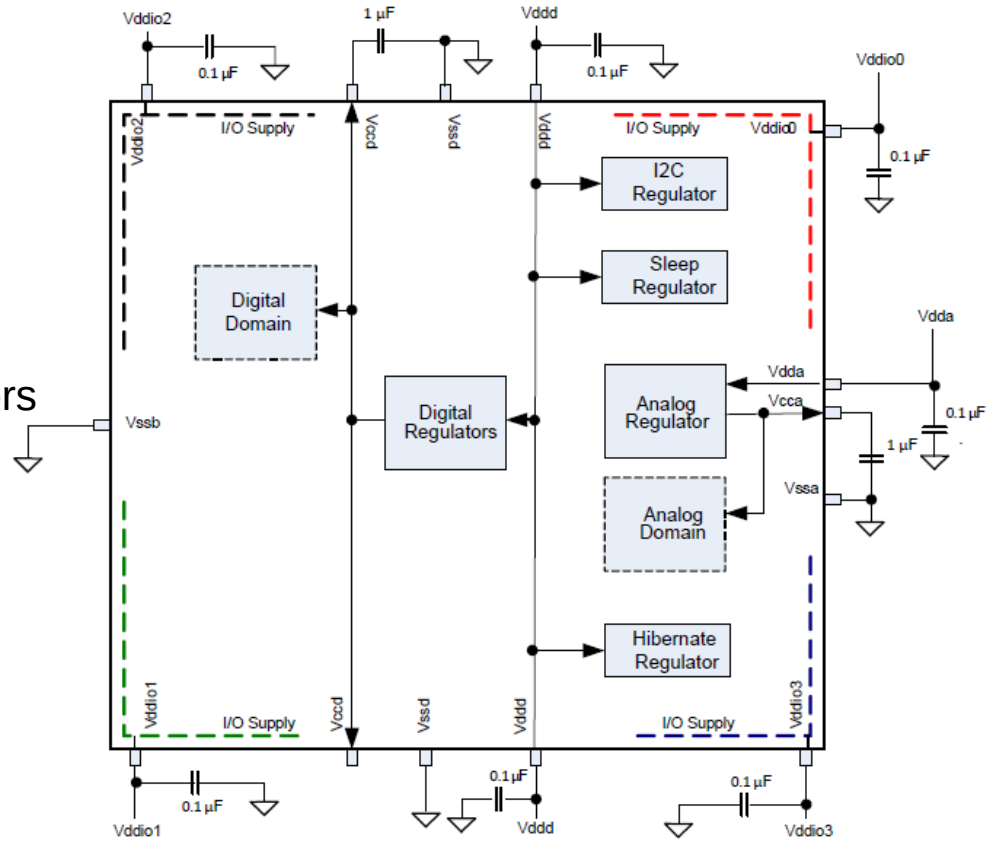
Power System and Supplies (no boost)

Standard Power Configuration

- No boost pump
- Vdda Vddd >= Vddio0/1/2/3
- Vdda = 1.8 – 5.5V

Supply Rules and Usage

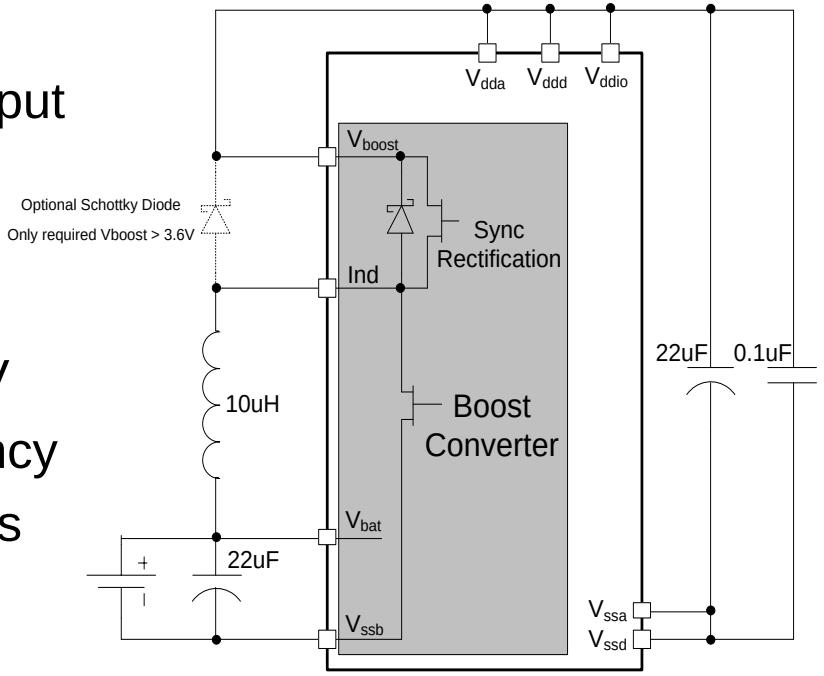
- Vdda: Must be highest voltage in system. Supplies analog high voltage domain and core regulator
- Vddd: Supplies digital system core regulators
- Vcca: Output of the analog core regulator. External 1 uF capacitance to ground is required.
- Vccd: Output of the digital core regulator. External 1 uF capacitance to ground is required. Both Vccd pins must be tied together on the PCB and share the 1 uF capacitance to ground
- Vddio0/1/2/3: Independent I/O supplies. May be any voltage in the range of 1.8V to Vdda



Power System (with boost)

Boost Converter Configuration

- Used to generate up to 5.0 V (Vout)
- Battery voltage as low as 0.5 V(Vbat)
- Output voltage and current limit based on input voltage and boost ratio
- 75 mA max current
- 0.5 – 3.6 V Vbat provides 1.8 – 5.0 V Vout
- Schottky diode required when Vout is > 3.6V
- Synchronous rectification maximizes efficiency
- Boost may be used to power external circuits



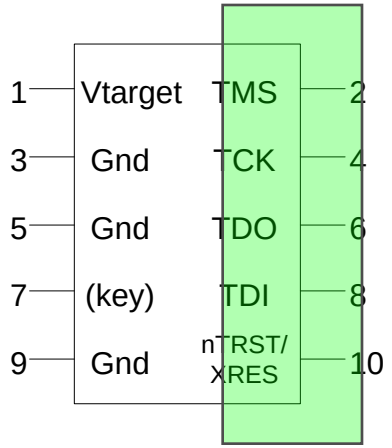
If boost not used

- Vssb, Vbat and Vboost must be tied to ground
- Ind left floating

Programming and Debug Interfaces

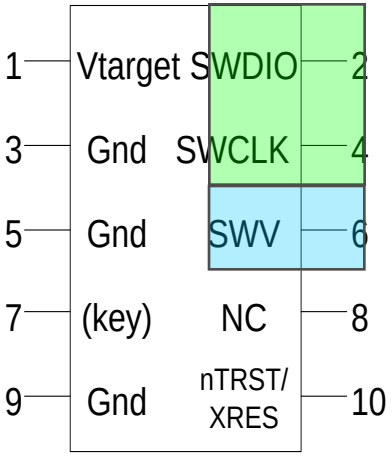
JTAG

- 4/5-wire Interface
- Supports all programming and debug features



Serial Wire Debug (SWD)

- Standard 2-wire interface for all CY tools and kits
- Supports all programming and debug features with same performance of JTAG
- Default debug interface in PSoC Creator



Programming and General Features

Flash operations

- Erase all
- Erase block – 256 blocks per device, independent of Flash size
- Program block
- Set block security
  - Unprotected – No protection
  - Factory Upgrade – Prevents external read
  - Field Upgrade – Prevents external read and write
  - Full Protection – Prevents external read and write as well as internal write

General Features available through JTAG/SWD

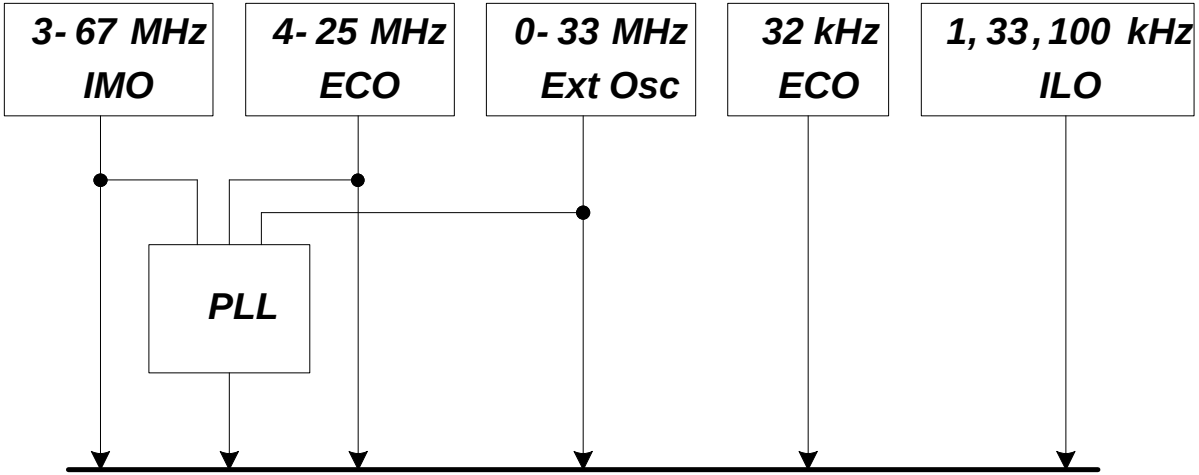
- I/O boundary scan through JTAG interface
- Enable/Disable JTAG and SWD interfaces
- On Chip Debug features enabled/disabled by firmware

Reset Sources

- IPOR – Initial Power on Reset
- XRES – External Reset
- PRES – Under Voltage on external supplies Vddd, Vdda (Precise Low Voltage Reset)
- PRES – Under Voltage on internal supplies Vccd, Vcca
- AHVI –Analog High Voltage Interrupt
- ALVI – Analog Low Voltage Interrupt
- DLVI – Digital Low Voltage Interrupt
- HRES – Hibernate mode under voltage detect
- SRES – User software and/or hardware generated reset
- WRES – Watchdog Timer reset
- JTAG or SWD interface generated reset

Clocking Sources

- Internal Main Oscillator (PSoC 3): 3-62 MHz (±1% at 3 MHz; ±7% at 62MHz)
- Internal Main Oscillator (PSoC 5LP): 3-62 MHz (±1% at 3 MHz; ±7% at 62MHz)
- PLL Output: 24 – 67 MHz
- External clock crystal input: 4 - 25 MHz
- External clock oscillator inputs: 0 - 33 MHz
- Clock doubler output: 12 - 48 MHz
- Internal Low speed Oscillator: 1 kHz, 33 kHz and 100 kHz
- External 32 kHz crystal input for RTC

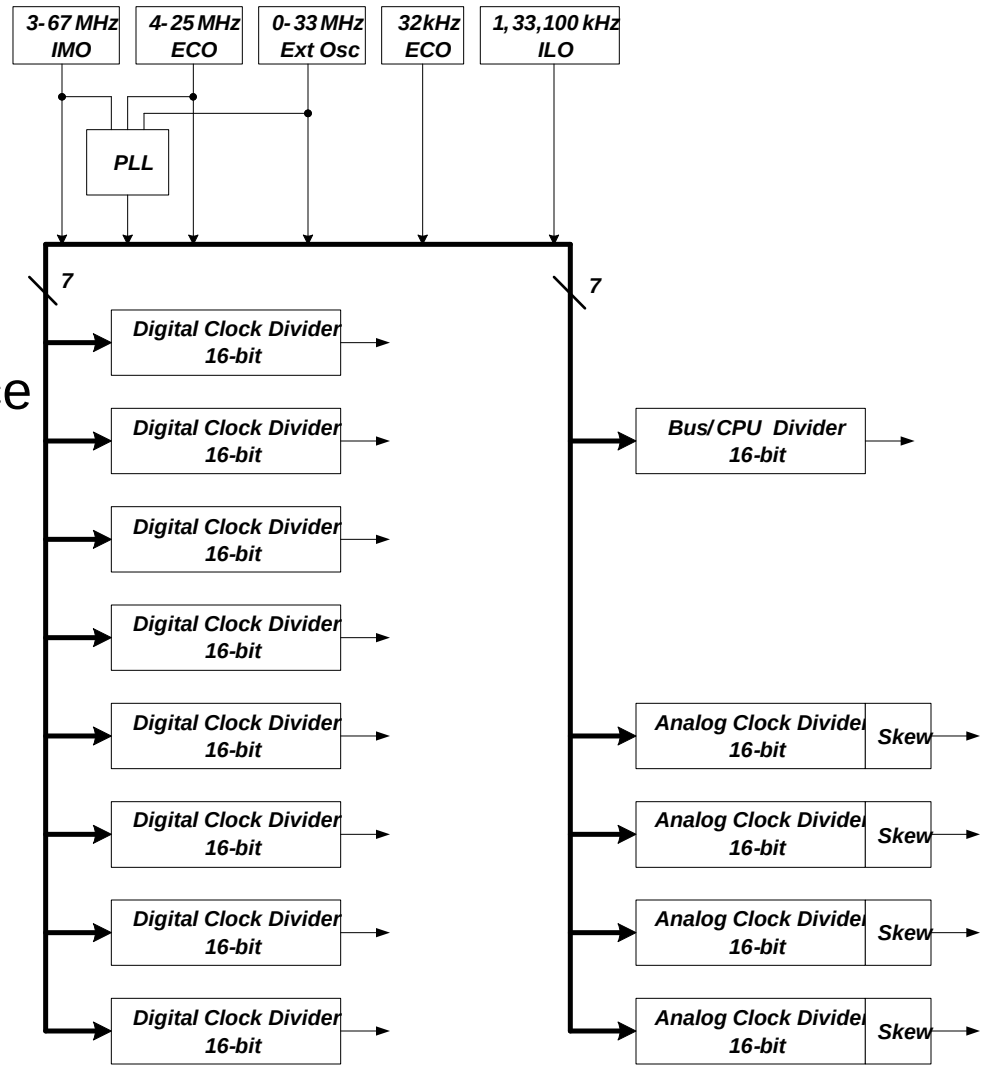


Clock Distribution

Clock Dividers

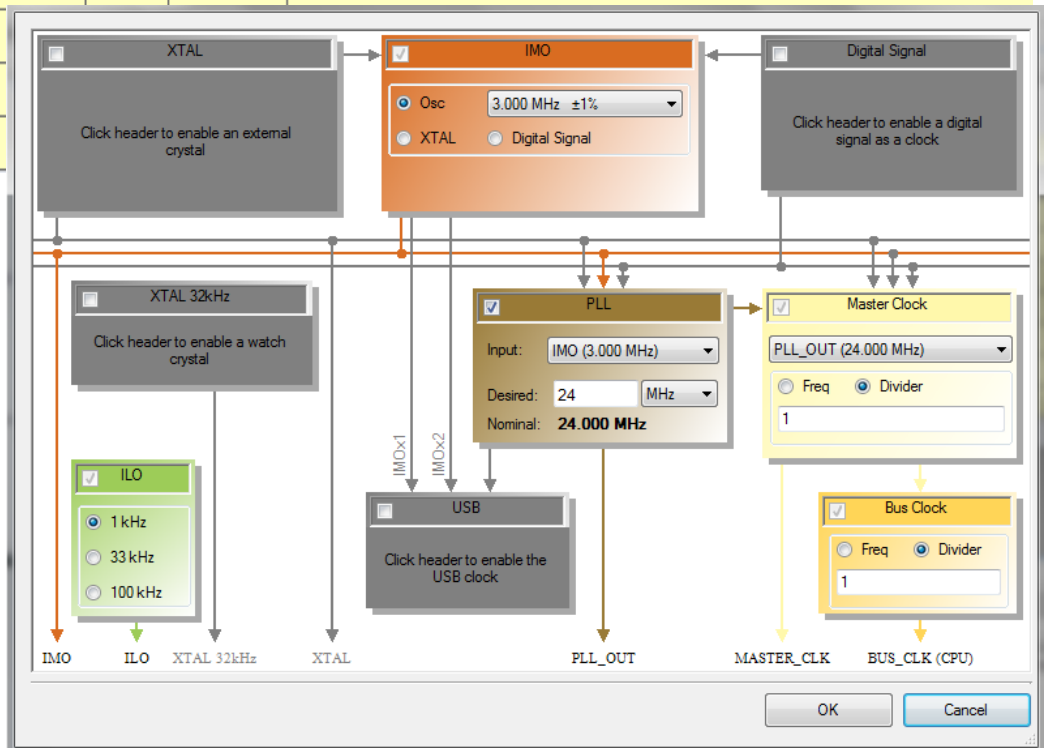
- 16-bit dividers
- 8 clock source inputs
- 8 digital domain clock dividers
- 4 analog domain clock dividers
  - Provide skew control to reduce digital switching noise
- 1 CPU divider

UDB's can be used to create additional digital clocks



System Clock Setup

Type	Name	Domain	Desired Frequency	Nominal Frequency	Accuracy (%)	Tolerance (%)	Divider	Start on Reset	Source Clock
System	USB_CLK	DIGITAL	48.000 MHz	? MHz	±0	-	1	☐	IMOx2
System	Digital Signal	DIGITAL	? MHz	? MHz	±0	-	0	☐	
System	XTAL 32kHz	DIGITAL	32.768 kHz	? MHz	±0	-	0	☐	
System	XTAL	DIGITAL	33.000 MHz	? MHz	±0	-	0	☐	
System	ILO	DIGITAL	? MHz	1.000 kHz	-50, +100	-	0	☑	
System	IMO	DIGITAL	3.000 MHz	3.000 MHz	±1	-	0	☑	
System	BUS_CLK (CPU)	DIGITAL	? MHz	24.000 MHz	±1				
System	MASTER_CLK	DIGITAL	? MHz	24.000 MHz	±1				
System	PLL_OUT	DIGITAL	24.000 MHz	24.000 MHz	±1				



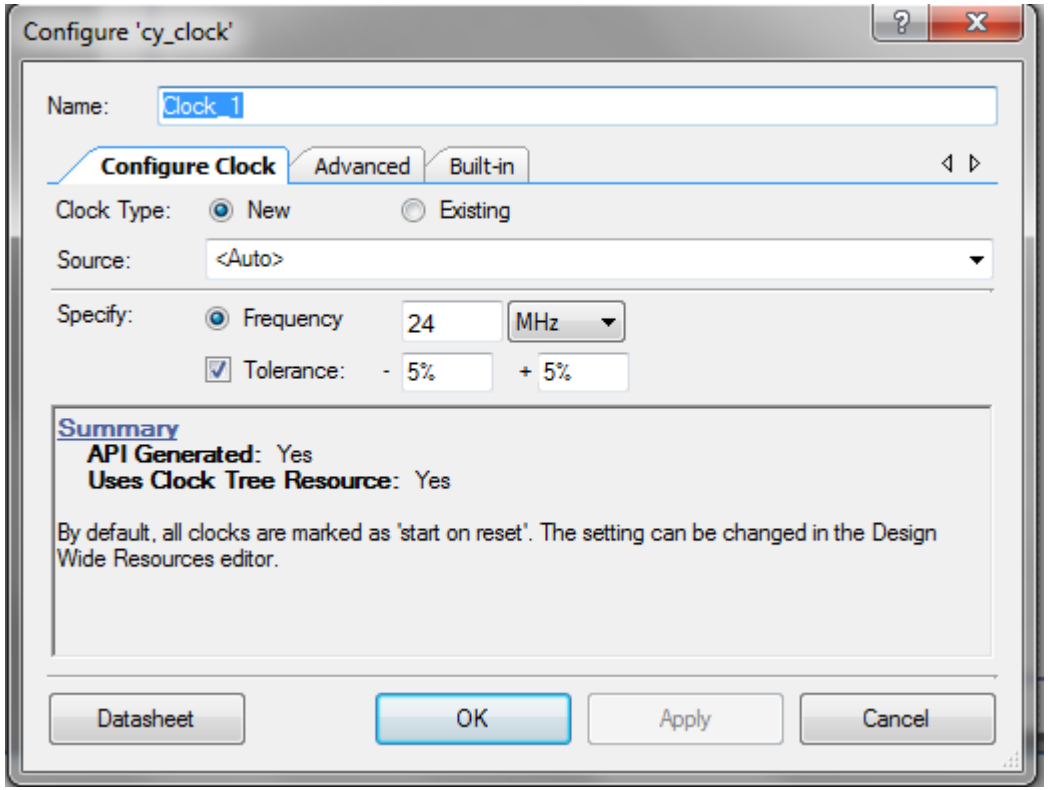
Easy to configure clock options using graphical configuration tool

Clock Management

Clocks allocated to dividers in clock tree

Clocks have software APIs to dynamically change frequency

Note: Reuse existing clocks to preserve resources



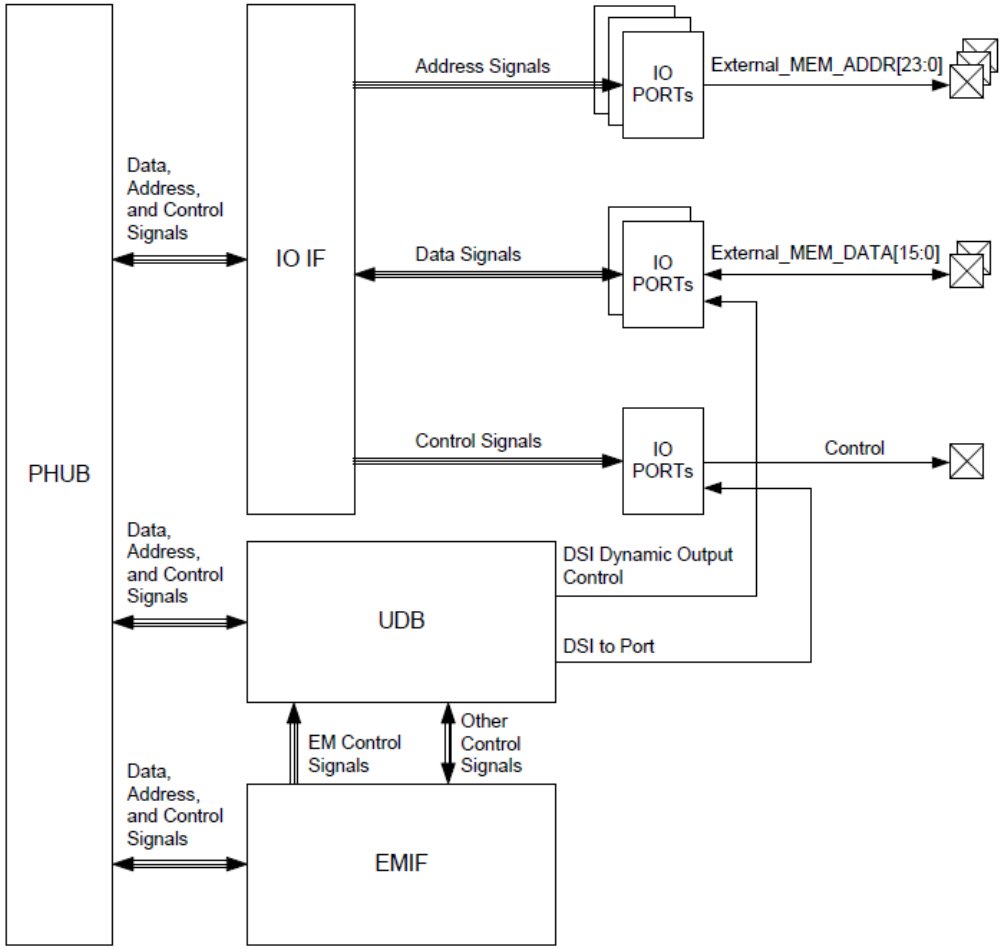
External Memory Interface (EMIF)

EMIF Supports:

- Sync SRAM
- Async SRAM
- Cellular RAM
- NOR Flash

EMIF Usage:

- Data only
- 8- or 16-bit data bus
- 8-, 16- or 24-bit address bus
- Max throughput 11-16 MHz depending on configuration details



Flash

Flash Blocks

- 256 blocks in all devices – 64 KB flash has 256-byte block size
- Each block may be set to 1 of 4 protection levels of increasing security
  - Unprotected – Allows internal and external reads and writes
  - Factory Upgrade – Prevents external read
  - Field Upgrade – Prevents external read and write
  - Full Protection – Prevents external read and write as well as internal write
- Flash is erased and programmed in block units

Specs

- Code executes out of Flash
- Flash-writes block CPU unless executing from cache
- 20 year minimum retention
- 10 K minimum endurance
- 15 ms block erase + write time

Error Correcting Code (ECC)

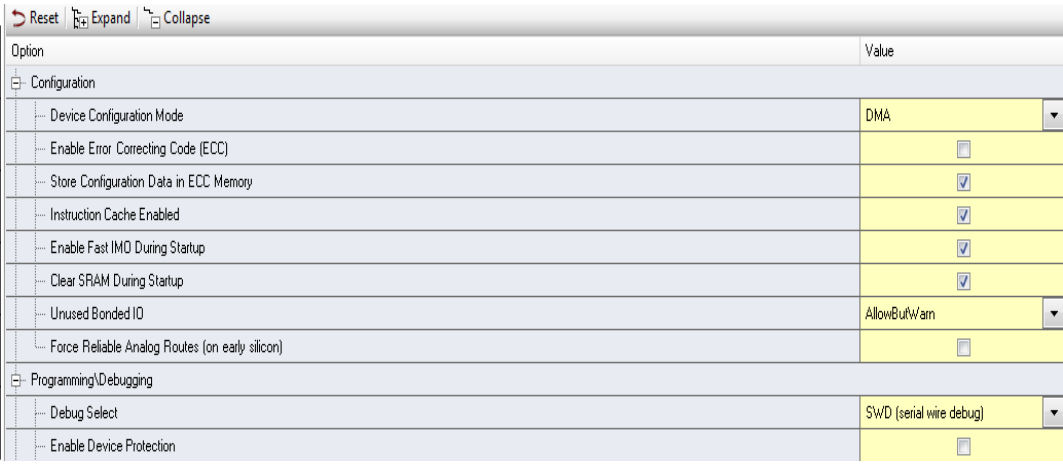
ECC = Flash Memory Error Correction

- Required for some high reliability designs (e.g. automotive and medical)
- Detects and corrects 1 bit of error per 8 bits
- Detects but does not correct 2 bits of error
- Correction is automatic; interrupt and flag bit are set
- 1 byte of ECC data for each 8 bytes of Flash data (1 row)
- 64 KB device includes + 8 KB of ECC memory for 72 KB total

8 KB is used for configuration data storage if ECC not used (default)

- ECC memory is mapped into contiguous region in peripheral space
- ECC memory may also hold user data
- Code cannot execute out of ECC memory

Byte	Byte	Byte	Byte	Byte	Byte	Byte	Byte	ECC
Byte	Byte	Byte	Byte	Byte	Byte	Byte	Byte	ECC
Byte	Byte	Byte	Byte	Byte	Byte	Byte	Byte	ECC
Byte	Byte	Byte	Byte	Byte	Byte	Byte	Byte	ECC
Byte	Byte	Byte	Byte	Byte	Byte	Byte	Byte	ECC
Byte	Byte	Byte	Byte	Byte	Byte	Byte	Byte	ECC



EEPROM

2 KB of EEPROM provided

Code cannot execute out of EEPROM

EEPROM Specs:

- EEPROM writes do not block CPU execution
- 20 year minimum retention
- 100K minimum endurance, 10M endurance at room temperature
- 10 ms single row erase + write cycle time
  - Supports single byte erase and writes (read / modify / write row)
  - May erase or write up to 16 consecutive bytes (1 row) at the same time

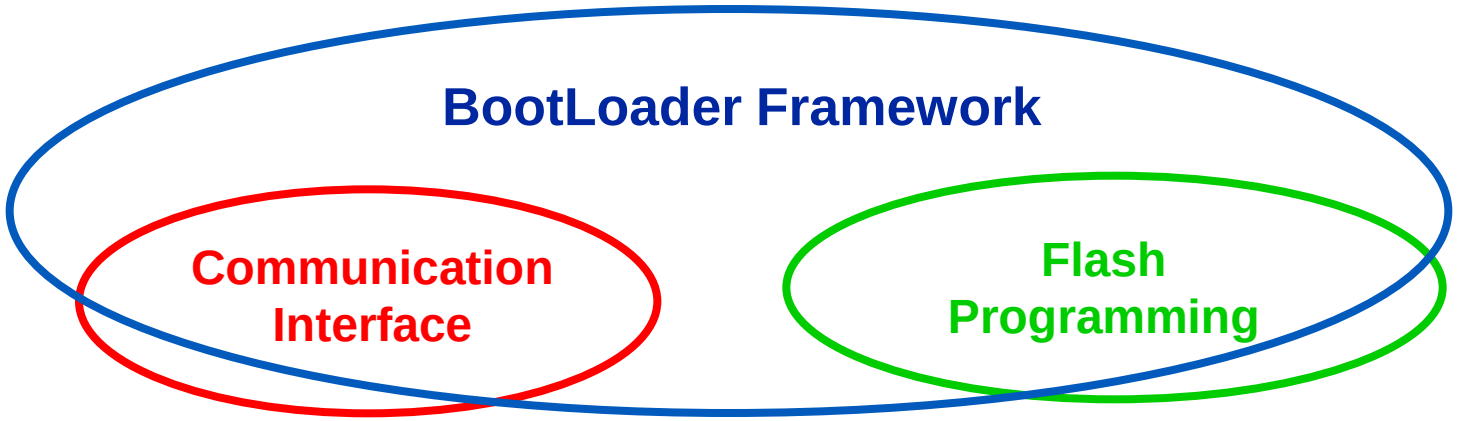
Bootloaders

Single Bootloader Supports

- I2C
- USB
- Others as required

Bootloader Integration

- Bootloader platform allows easy customization
- No bootloader programmed in parts at factory
- PSoC Creator integrates bootloader support seamlessly
- Bootloader is just another component



Direct Memory Access (DMA)

- 24 hardware channels
- 8 priority levels with minimum bandwidth guarantees

Priority	Minimum Guaranteed Bus Bandwidth
0	100%
1	100%
2	50%
3	25%
4	12.50%
5	6.30%
6	3.10%
7	1.50%

- 128 Transaction Descriptors (TD) tell channel what to do
  - 2kB of dedicated SRAM holds all TD data
- Multiple channels or TDs may be chained or nested
- Configurable burst size
- DMA between peripherals on same spoke limited to 1-byte burst length

GPIO - I/O Digital Features

Independent supply rails

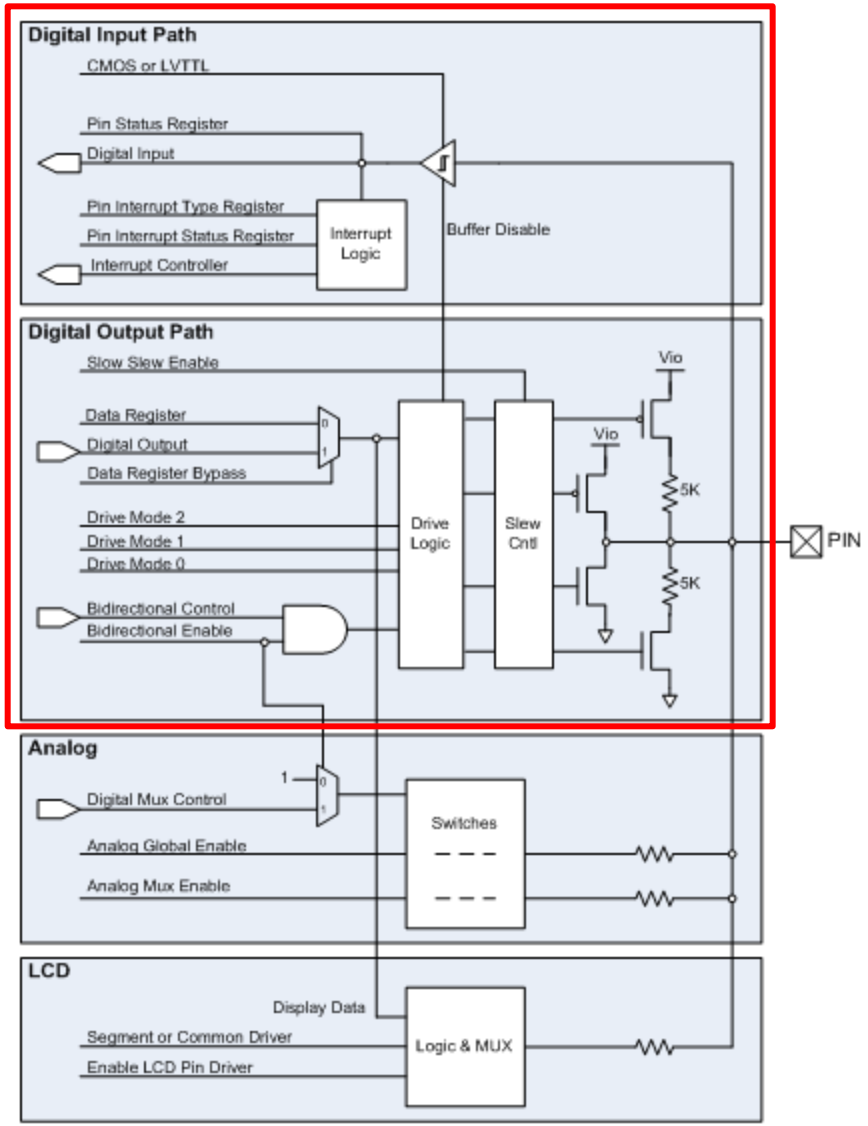
- Each quadrant of device has separate Vddio supply
- GPIO Vddio must be <=Vdda

Logic level maximum current

- 8 mA sink
- 4 mA source

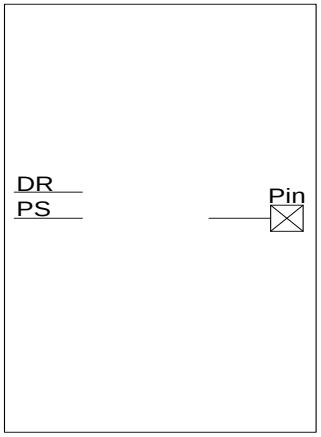
Pin maximum current

- ~25 mA sink
- ~25 mA source

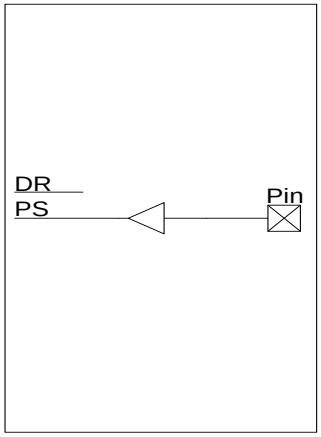


GPIO - I/O Digital Features

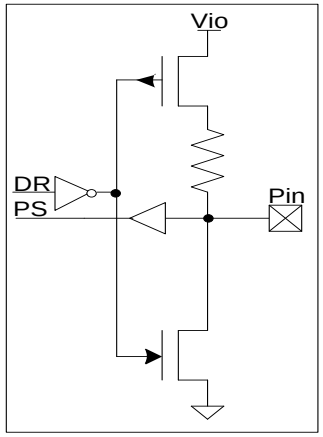
8 Drive Modes



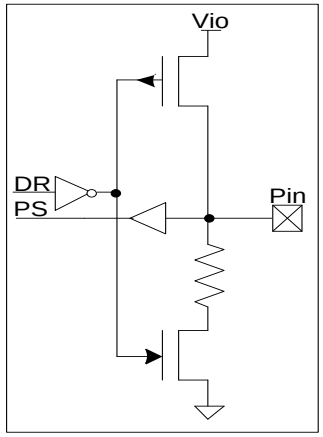
0. High Impedance Analog



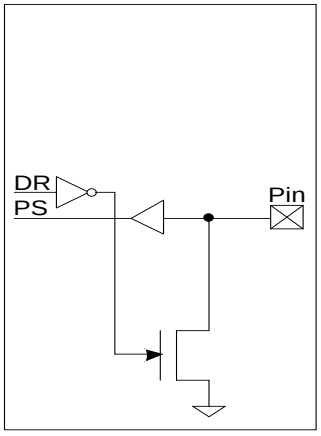
1. High Impedance Digital



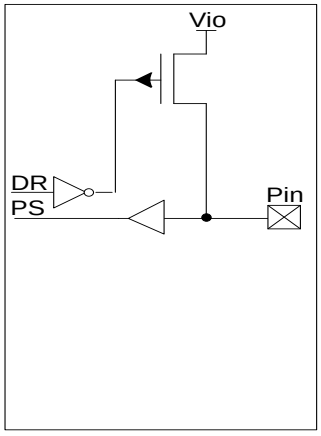
2. Resistive Pull-Up



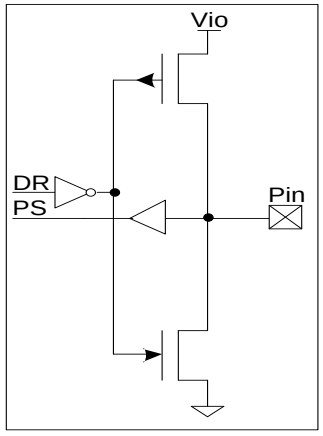
3. Resistive Pull-Down



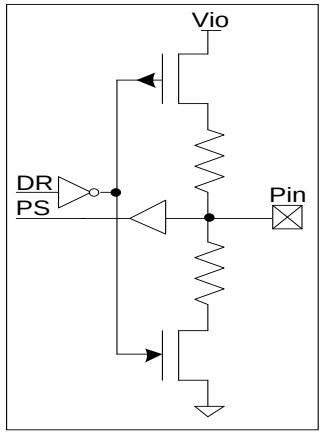
4. Open Drain, Drives Low



5. Open Drain, Drives High



6. Strong Drive



7. Resistive Pull-Up & Down

GPIO - Interrupts

Each GPIO port has:

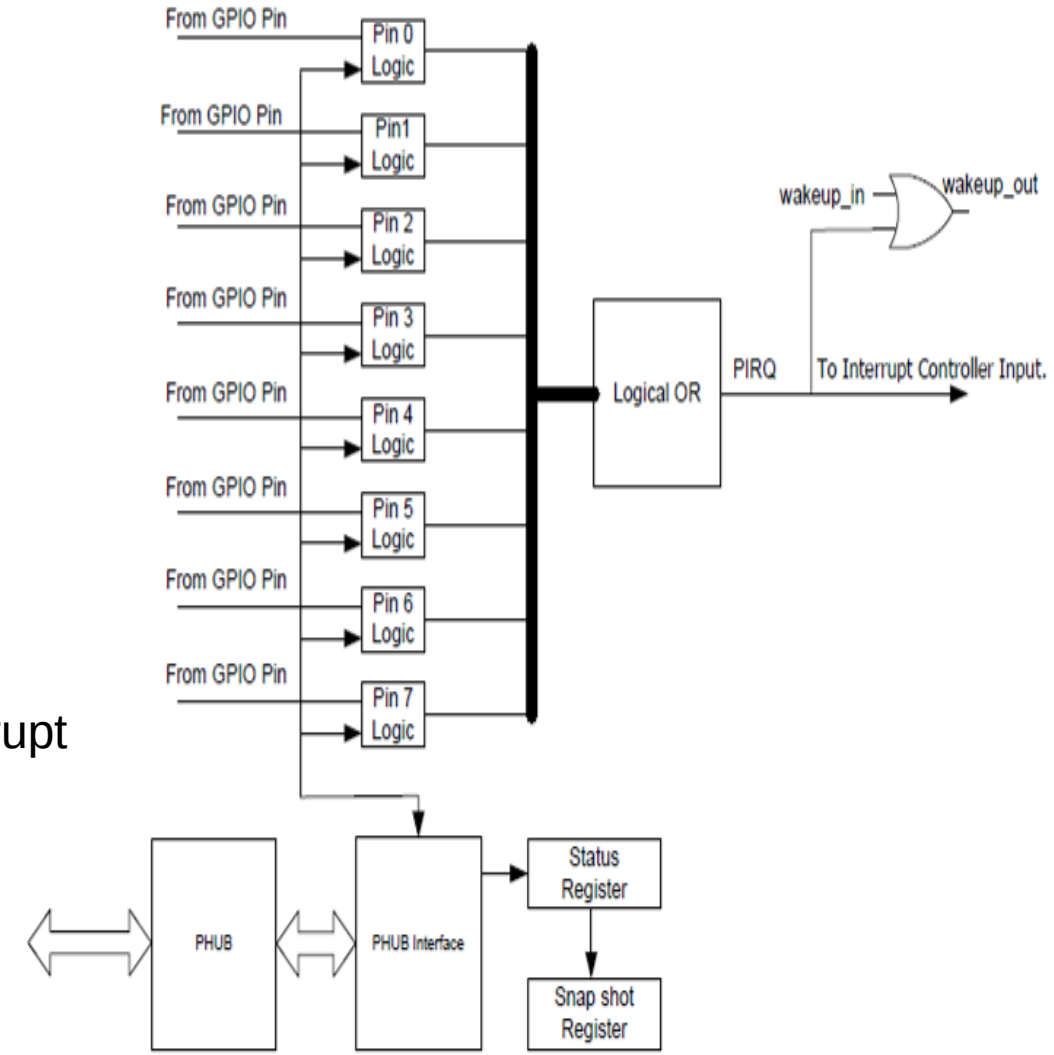
- Port Interrupt Control Unit (PICU)
- Dedicated Interrupt vector

Interrupt on:

- Rising edge
- Falling edge
- Any edge

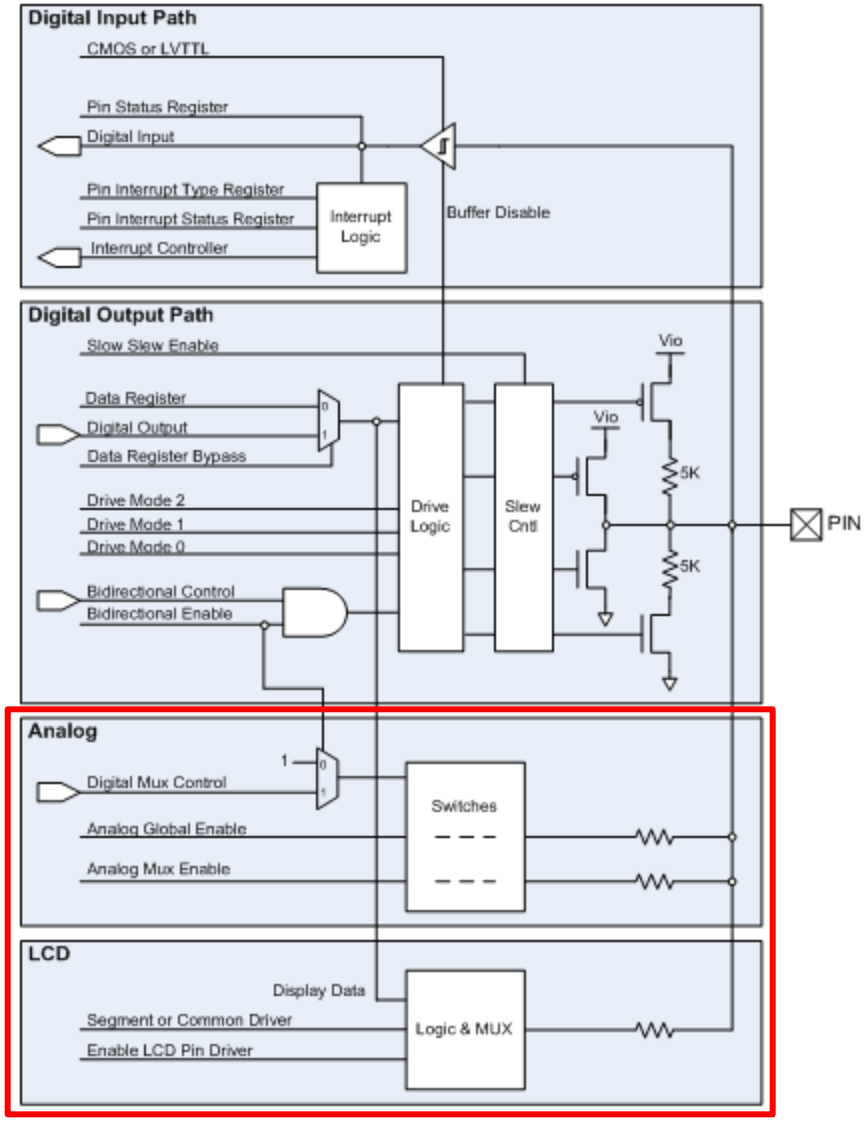
Status Register

- Latches which pin triggered interrupt
- Available for firmware read
- Read clear



GPIO - I/O Analog Features

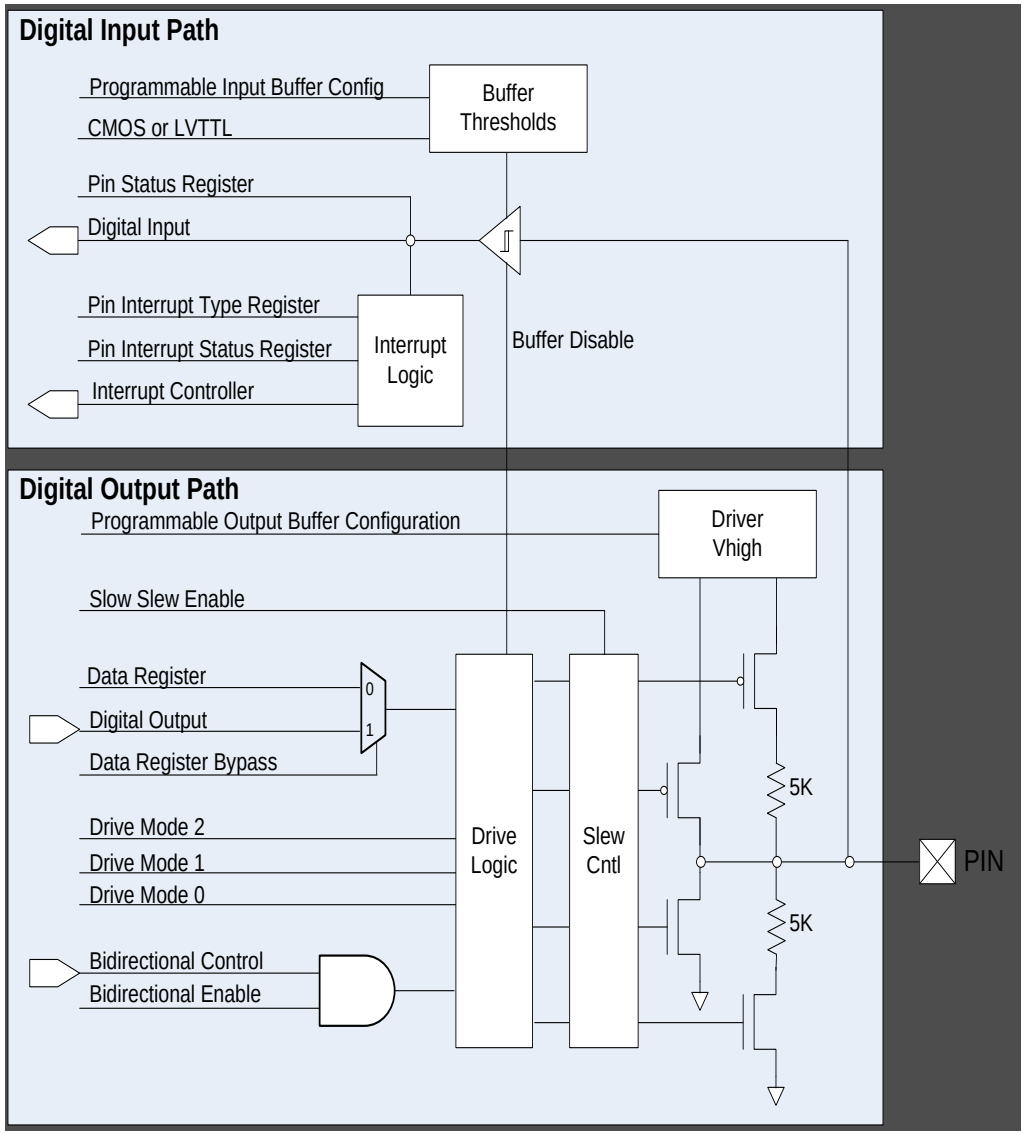
- All pins inputs and outputs
- Supports two independent analog connections at each pin
- CapSense Touch Sensing
- LCD char/segment drive
- Hardware controlled analog mux at pin
- Some pins have additional routing features:
  - OpAmps
  - High Current DAC mode



SIO (Special I/O) Features

Same as GPIO with exceptions:

- 5.5 V tolerant at all Vdda levels
  - Hot Swap
  - Overvoltage tolerance
- Configurable drive and sense voltage levels
  - Basic DAC output
  - High Speed CMP input
- Logic level max current
  - 25 mA sink
  - 4 mA source
- Pin max current
  - ~50 mA sink
  - ~25 mA source
- No Analog
- No LCD char/segment drive
- No CapSense touch sensing

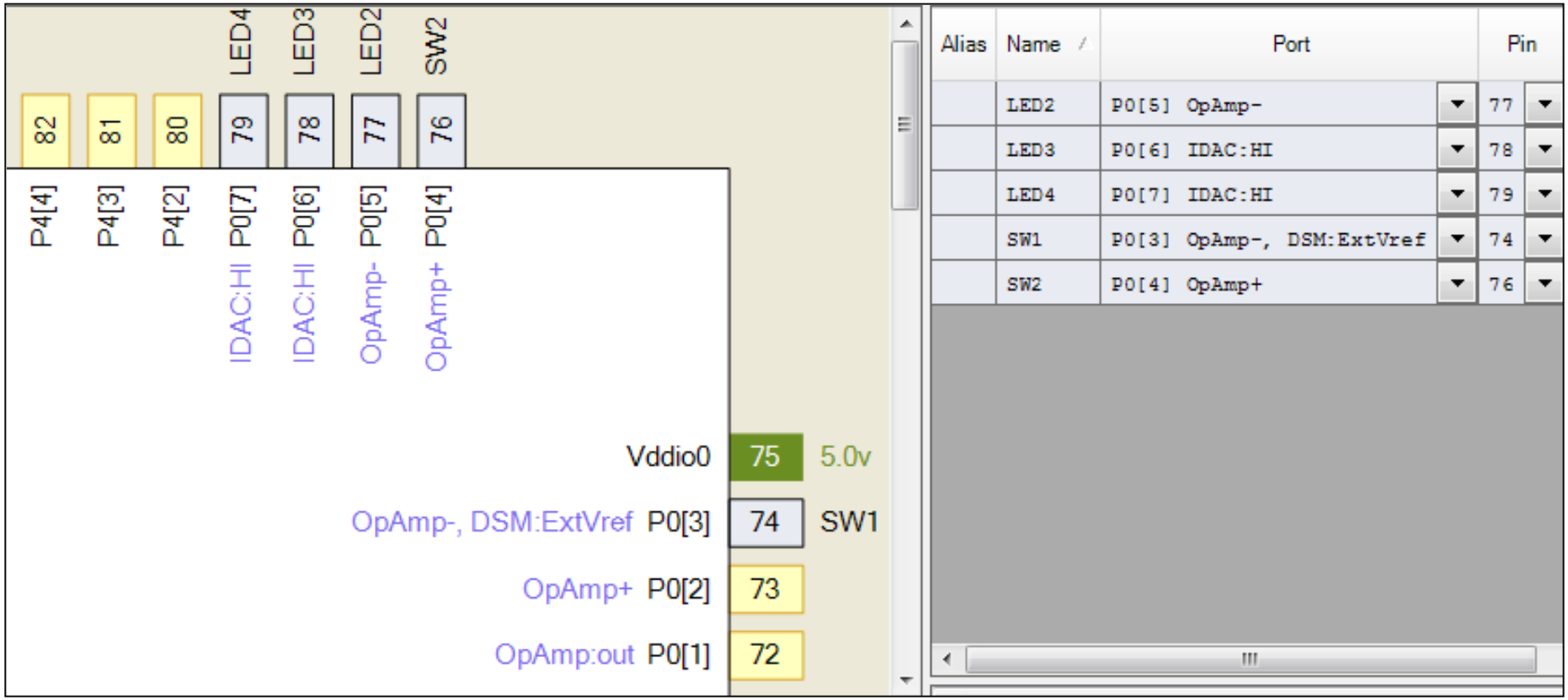


Pin Management

PSoC Creator can select pins automatically

- Lock pins when device pin out is finalized

Manual override in DWR file



Interrupts

Interrupt Controller

- 32 interrupt vectors
- Dynamically adjustable vector addresses
- 8 priority levels
- Each vector supports one of these sources
  - Fixed function DMA, DSI (UDB) route

PSoC 8051

- 32 interrupt vectors vs. standard 8051 is five

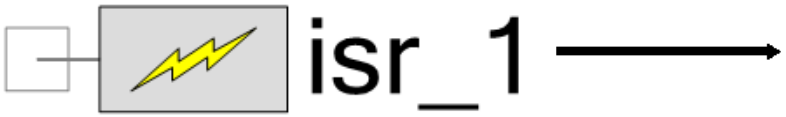
ARM Cortex-M3

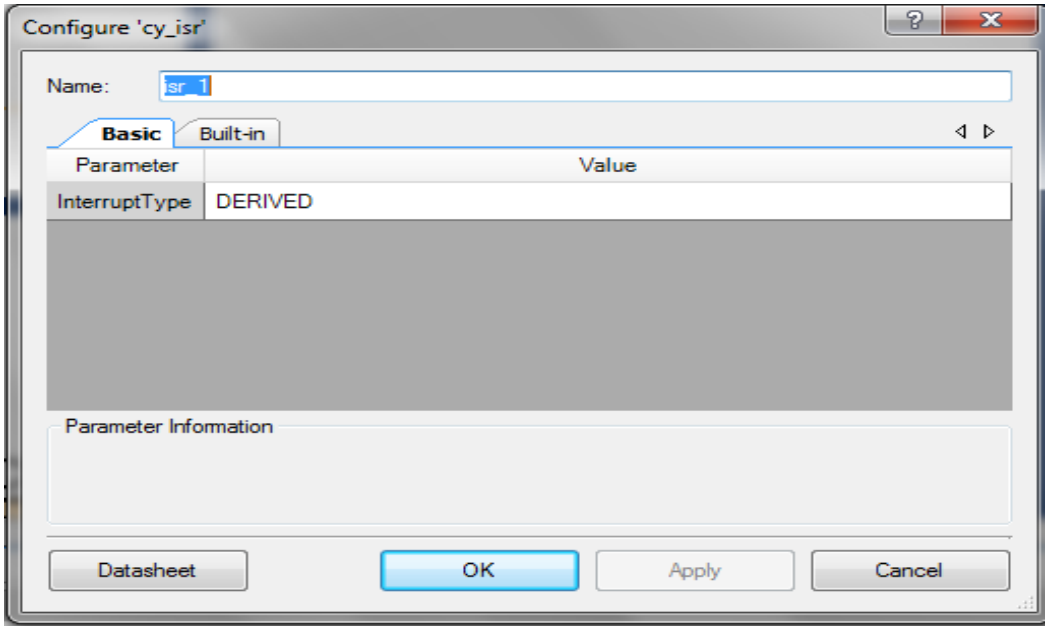
- 32 interrupts + 15 exceptions
- Tail chaining

Int #	Fixed Function	DMA	UDB
0	LVD	DMA output	UDB signal (DSI)
1	ECC	DMA output	UDB signal (DSI)
2	Boost Buck	DMA output	UDB signal (DSI)
3	Sleep (Pwr Mgr)	DMA output	UDB signal (DSI)
4	PICU[0]	DMA output	UDB signal (DSI)
5	PICU[1]	DMA output	UDB signal (DSI)
6	PICU[2]	DMA output	UDB signal (DSI)
7	PICU[3]	DMA output	UDB signal (DSI)
8	PICU[4]	DMA output	UDB signal (DSI)
9	PICU[5]	DMA output	UDB signal (DSI)
10	PICU[6]	DMA output	UDB signal (DSI)
11	PICU[7]	DMA output	UDB signal (DSI)
12	PICU[8]	DMA output	UDB signal (DSI)
13	Comparator Int	DMA output	UDB signal (DSI)
14	Switched Cap Int	DMA output	UDB signal (DSI)
15	I2C	DMA output	UDB signal (DSI)
16	CAN	DMA output	UDB signal (DSI)
17	Timer/Counter0	DMA output	UDB signal (DSI)
18	Timer/Counter1	DMA output	UDB signal (DSI)
19	Timer/Counter2	DMA output	UDB signal (DSI)
20	Timer/Counter3	DMA output	UDB signal (DSI)
21	USB SOF Int	DMA output	UDB signal (DSI)
22	USB Arb Int	DMA output	UDB signal (DSI)
23	USB Bus Int	DMA output	UDB signal (DSI)
24	USB Endpoint[0]	DMA output	UDB signal (DSI)
25	USB Endpoint[1]	DMA output	UDB signal (DSI)
26	USB Endpoint[2]	DMA output	UDB signal (DSI)
27	USB Endpoint[3]	DMA output	UDB signal (DSI)
28	USB Endpoint[4]	DMA output	UDB signal (DSI)
29	DFB Int	DMA output	UDB signal (DSI)
30	Decimator Int	DMA output	UDB signal (DSI)
31	Reserved	DMA output	UDB signal (DSI)

Interrupt Component

GUI-based Configuration





API

isr_1_Start() – Configures and enables the interrupt.

Typically the only API required to be called

Advanced APIs

isr_1_SetVector()	isr_1_GetState()
isr_1_SetPriority()	isr_1_Disable()
isr_1_GetPriority()	isr_1_SetPending()
isr_1_Enable()	isr_1_ClearPending()

Review

You should now be able to:

- Understand the system block diagram of PSoC 3 / PSoC 5LP devices
- Understand and use the PSoC 3 / PSoC 5LP System Resources, including:
  - Power system
  - Programming and debugging
  - Configuration and boot process
  - Resets
  - Clocking
  - Memory and Mapping
  - DMA and PHUB
  - I/O
  - Interrupts

INTRODUCTION TO PSOC 3 AND PSOC 5LP

DIGITAL PERIPHERALS

Section Objectives

At the end of this section you should be able to:

- Understand Universal Digital Blocks (UDBs) in PSoC 3 / PSoC 5LP
- Use and implement digital peripherals with PSoC Creator

Digital Subsystems

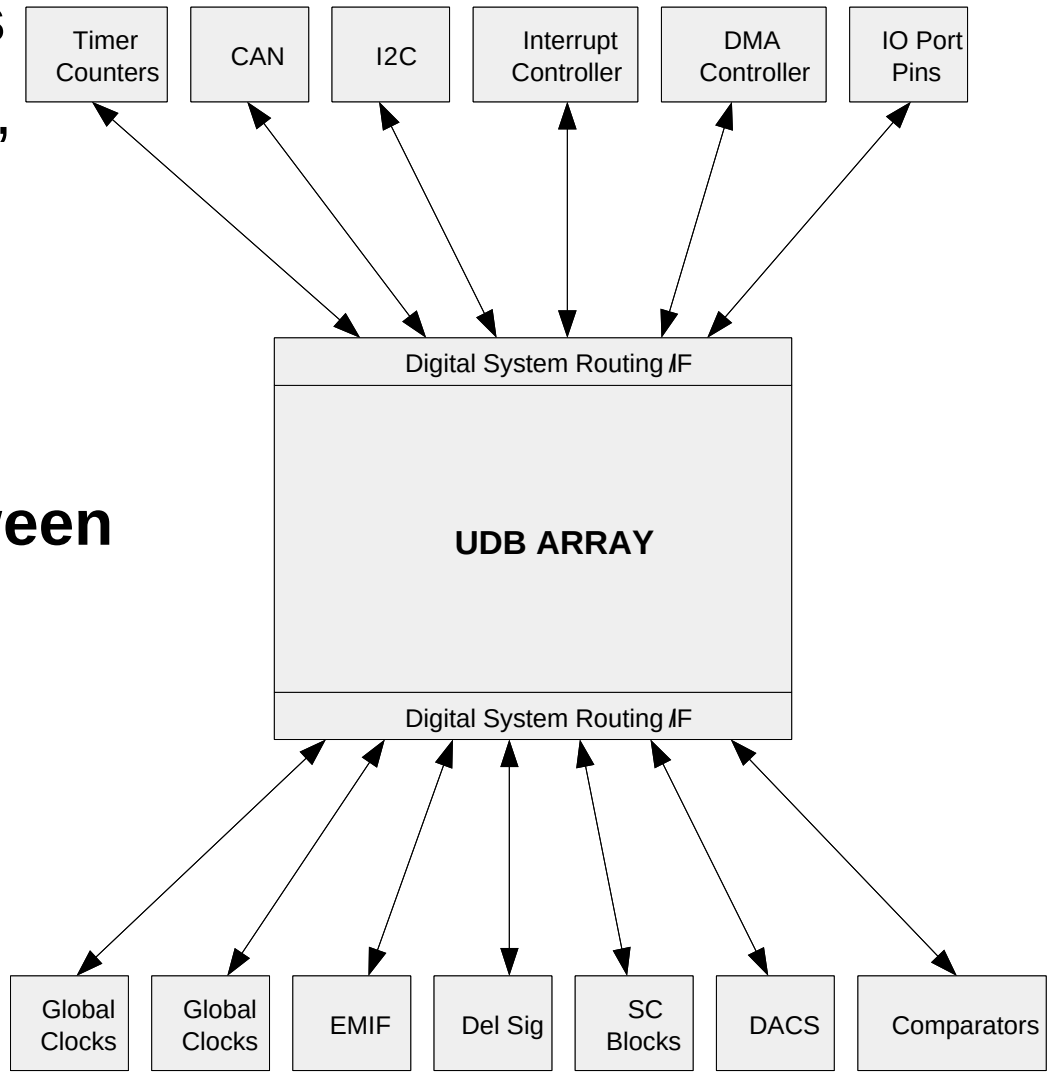
Fixed-function Peripherals

- Counter/Timer/PWMs, I2C, USB, CAN

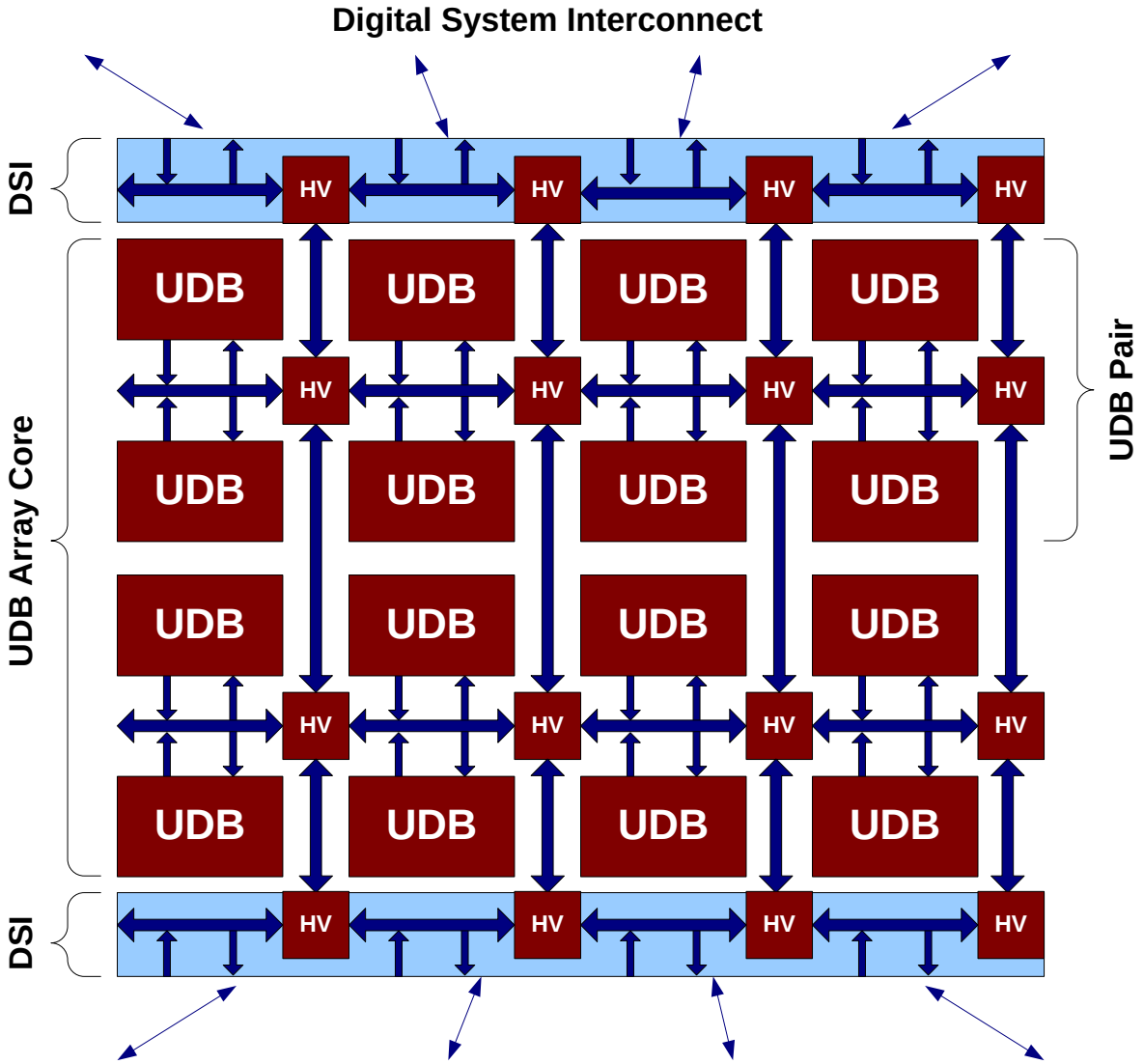
Universal Digital Blocks

Digital Interconnects Between

- Clocks
- IO pins
- Interrupts
- DMA
- External Memory
- Analog system



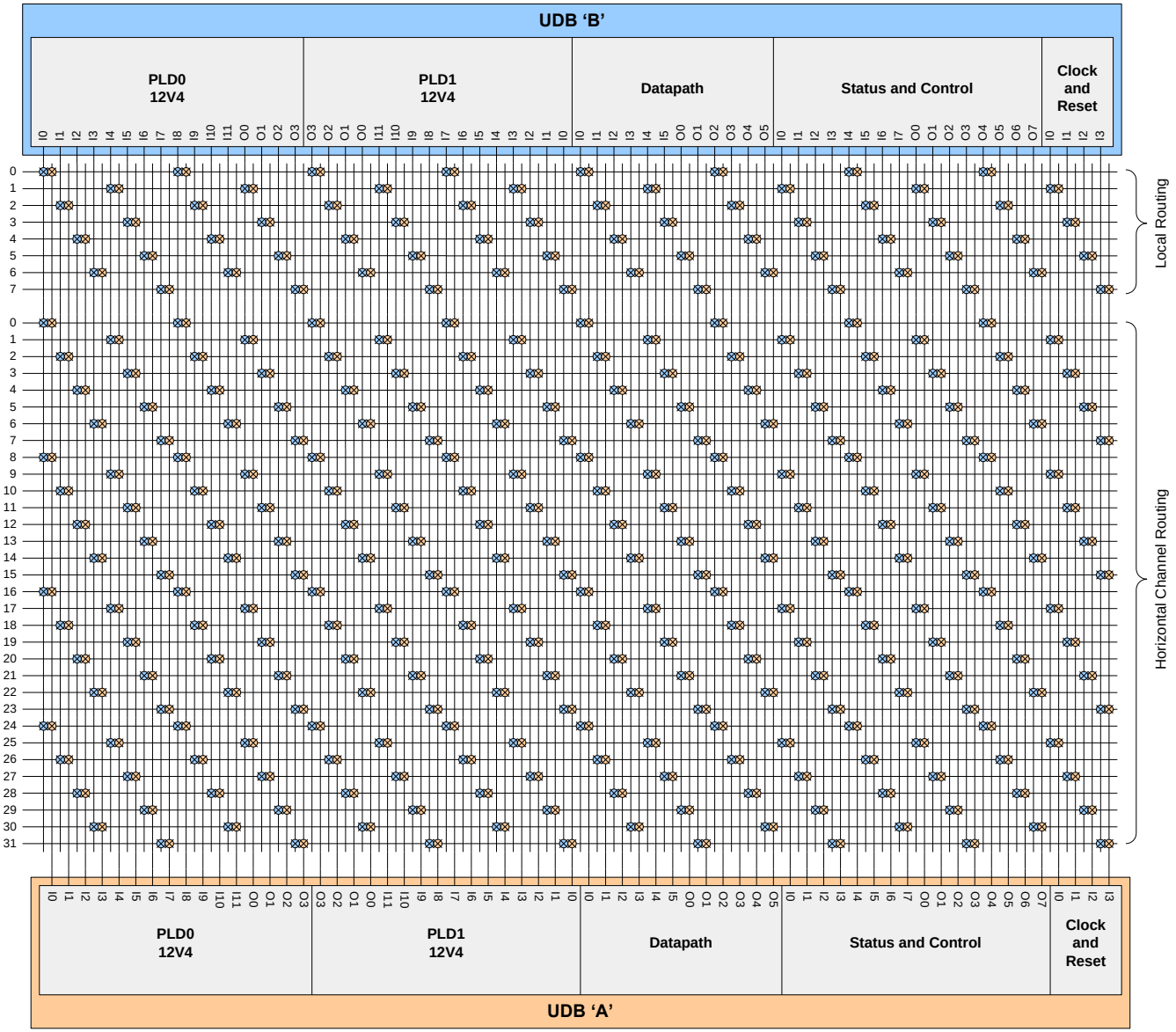
UDB Array


Digital System Interconnect
DSI
HV
UDB
UDB Array Core
UDB Pair
DSI
HV – Horizontal/Vertical Routing Interconnects
Digital System Interconnect

Digital Signal Interconnects (DSI)

Routing Example:

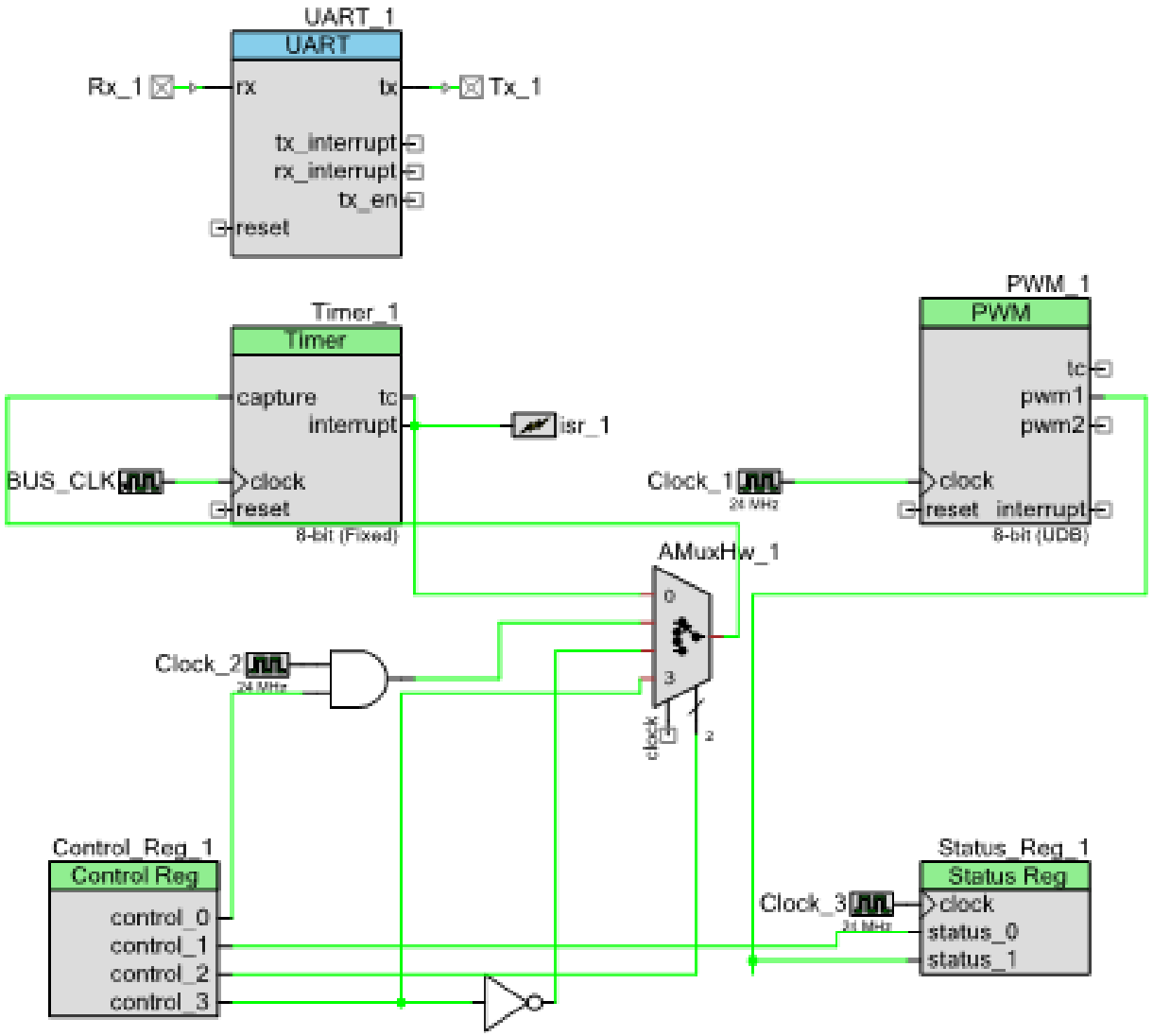
- Single UDB Pair
- 7000 DSI registers



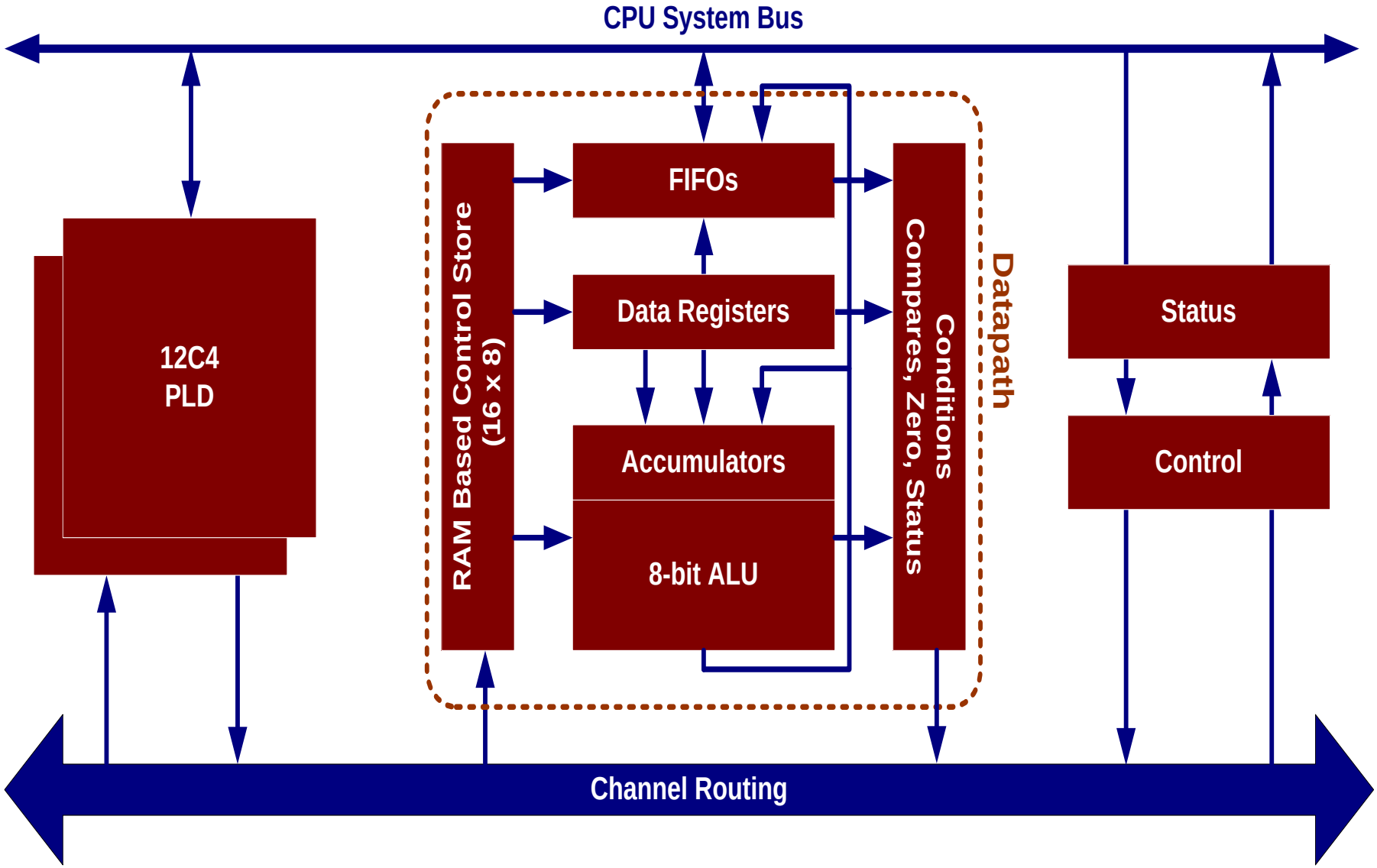
DSI, Automated

PSoC Creator enables:

- Schematic entry
- Automatic place and route
- Optimizations for analog and digital routing



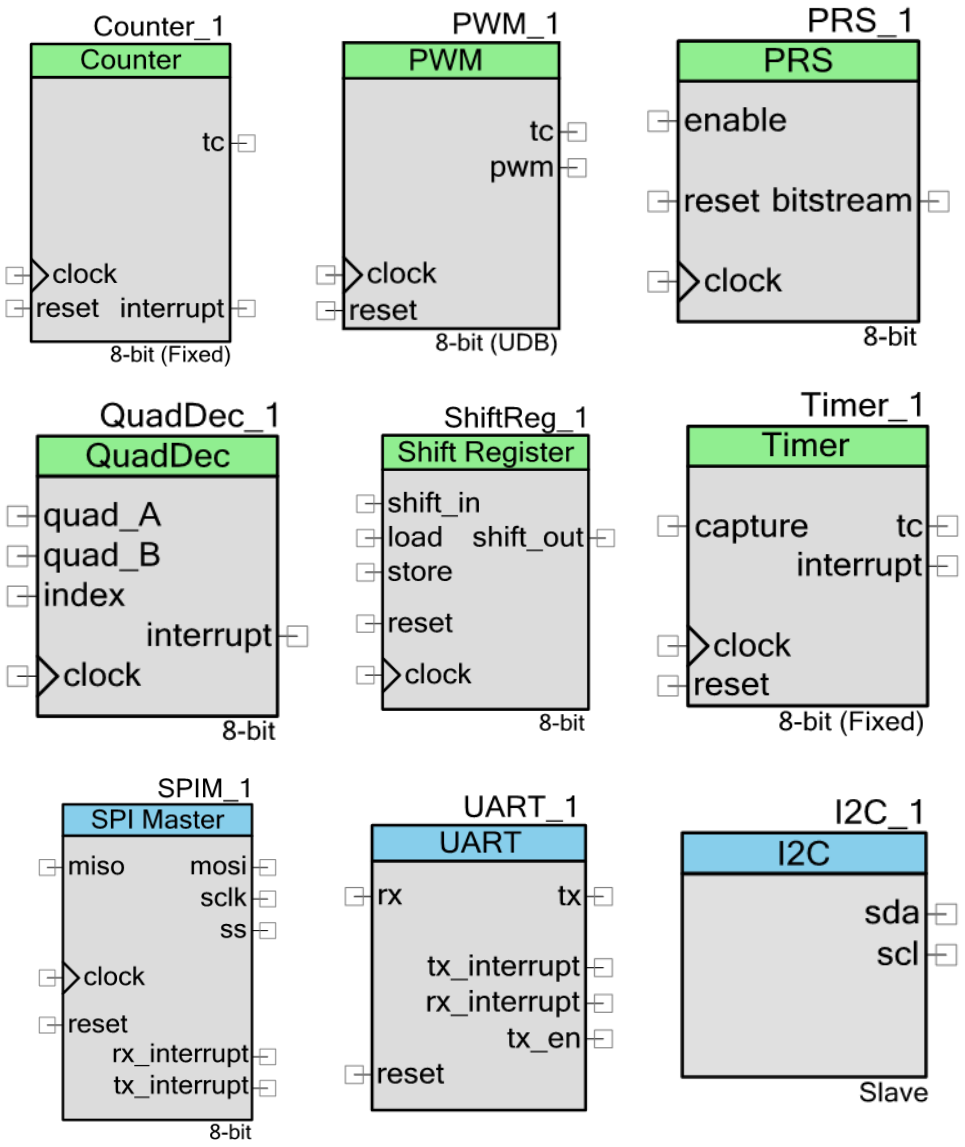
UDB Block Diagram



Digital Peripherals

Sample of Digital Peripherals:

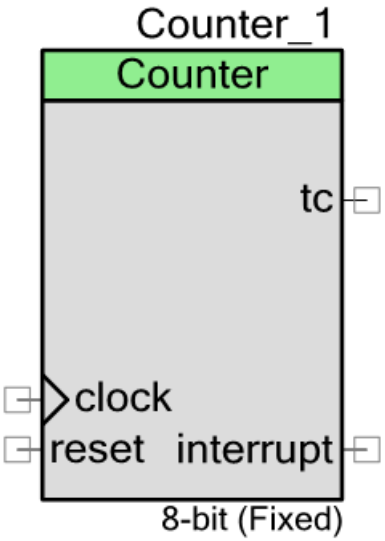
- Counter
- Timer
- PWM
- PRS
- I2C
- USB
- UART
- SPI
- CAN
- Char/Segment LCD Drive



Counter

Fixed/UDB Counters:

- General-Purpose counter
- Continuous, reload on reset, terminal count, or one shot mode
- Compare options: < <= > >= =
- Enable, reset, capture inputs
- Compare, TC, interrupt outputs
- Interrupts on various events



Fixed-Function Counters:

- 4 Available
- 8- or 16-bit
- Down counter only
- Single capture register

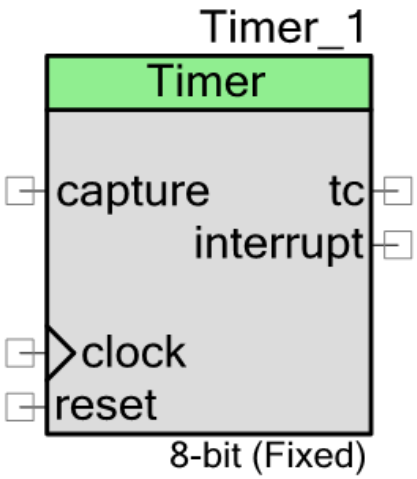
UDB-Based:

- 8-, 16-, 24- or 32-bit
- Many options:
  - Enable, count, capture, compare
  - 4-deep capture FIFO

Timer

Fixed/UDB Timers:

- General-Purpose timer for measuring time between H/W events
- Capturing times of events
- Periodic pulse or interrupt
- Continuous, reload on reset, terminal count or one shot mode
- Enable, reset, capture and trigger inputs
- Compare, terminal count, interrupt outputs
- Interrupts on various events



Fixed-Function Counters:

- 4 Available
- 8- or 16-bit
- Capture on rising edge only
- Single capture register

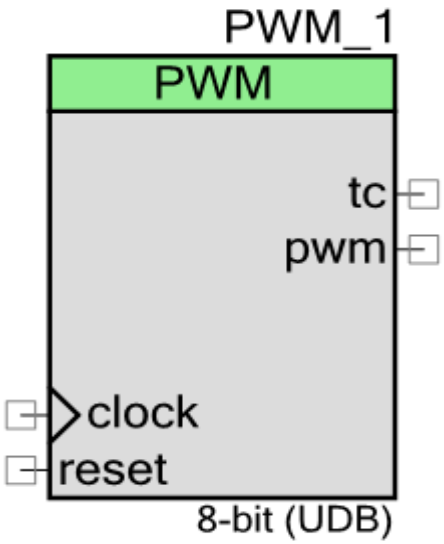
UDB-Based:

- 8-, 16-, 24- or 32-bit
- Many options:
  - Enable, trigger, capture
  - Capture counter and capture interrupt CTs
  - 4-deep capture FIFO

PWM

Fixed/UDB PWMs:

- General-Purpose PWM for motor control, LED brightness, etc.
- 8- or 16-bit
- Compare options: < <= > >= =
- Configurable deadbands
- Enable, trigger and kill inputs
- Biphase, TC and interrupt outputs
- Interrupts on various events



Fixed-Function PWMs:

- 4 Available
- 1 PWM output
- Left-aligned
- Hardware deadband and output kill

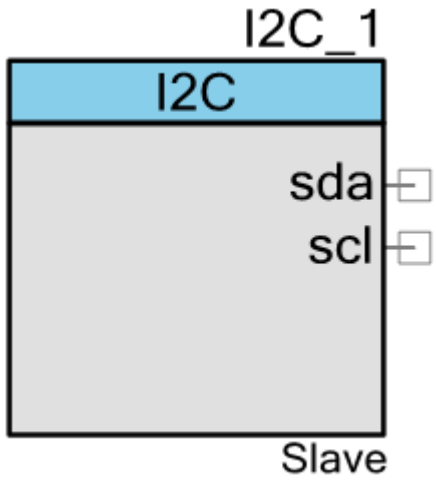
UDB-Based:

- 1 or 2 PWM outputs
- Left, right, center or dual-edge align
- Many options:
  - Enable, trigger, kill and compare

I2C

Fixed/UDB I2Cs:

- I2C slave, master or multi-master
- Hardware or firmware address decode
- 7- or 10-bit addressing (10-bit F/W only)
- Bus stalling / clock stretching
- SMBus, PMBus supported
- Routes SDA/SCL to any GPIO/SIO pins
- Interrupts for variety of bus events



Fixed-Function I2C:

- 1 Available
- Standard 100 Kbps or Fast 400 Kbps
- Responds Sleep Low-Power mode if dedicated SIO connections used

UDB-Based:

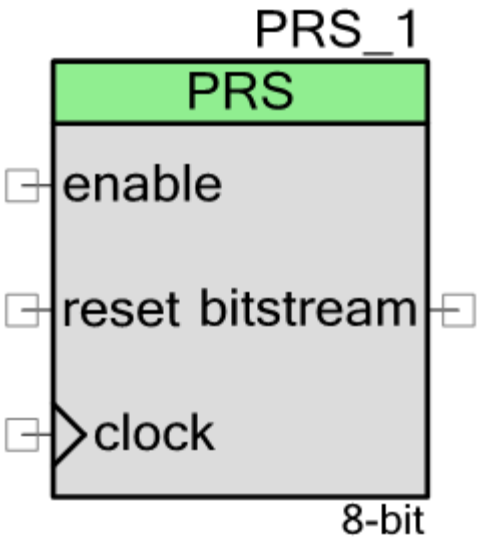
- Adds high-speed mode; up to 3.4 Mbps

Pseudo Random Sequencer

Pseudo Random Sequencer (PRS)

Specs:

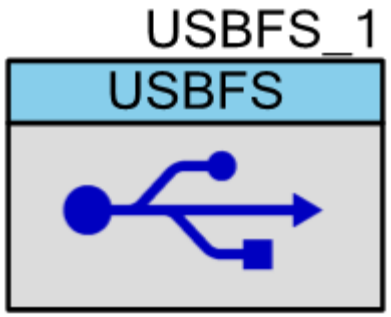
- 2- to 64-bit sequence length
- Serial output bit stream
- Continuous or single step run modes
- Standard or custom polynomial
- Standard or custom seed value
- Enable input provides synchronized operation with other components
- Computed pseudo-random number can be read directly from the linear feedback shift register (LFSR)



USB

Specs:

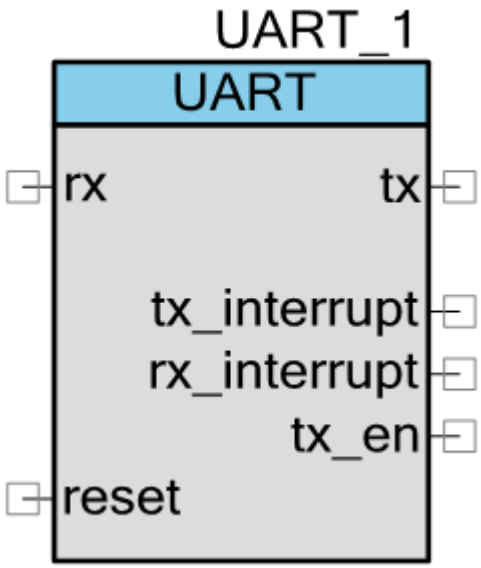
- Fixed-function, USB 2.0 Full Speed (12 Mbps) peripheral
- 8 unidirectional endpoints
- Shared 512 byte buffer
- Transfer Types: Control, Interrupt, Bulk, Isochronous
- DMA access / capable
- Wake from sleep
- *Example uses: HID, Virtual Comm Port*



UART

Specs:

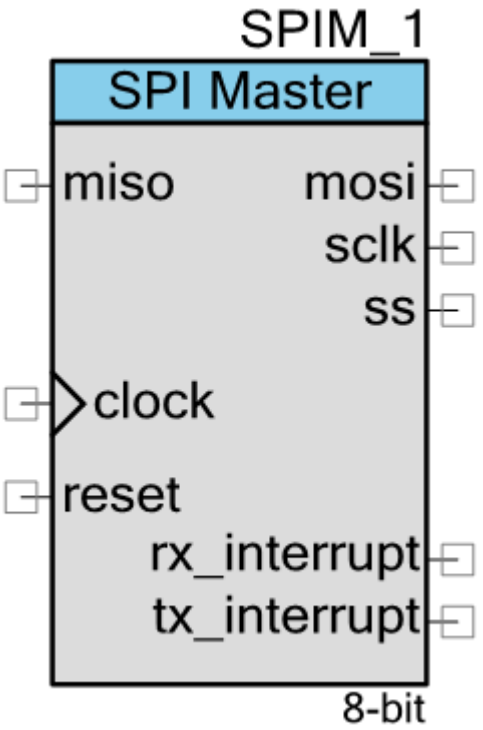
- Full-Duplex, Tx only and Rx only
- 5- to 9-data bits
- 110- to 921600-bps or arbitrary up to 4 Mbps
- Rx and Tx buffers 1- to 255-bytes
- Framing, Parity and Overrun error detection
- 9-bit address mode with hardware address detection
- Optional Tx enable for RS-485



SPI

Specs:

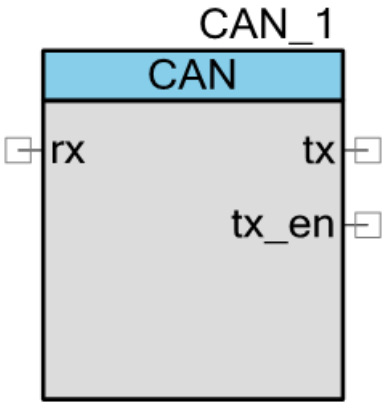
- Master or Slave
- Data rates to 33 Mbps
- 2- to 16-bit data width
- 4 SPI modes
- LSB or MSB first
- 1- to 255-byte Rx and Tx buffers
- Hardware Slave Select generation
- Supports 3-wire mode



CAN

Specs:

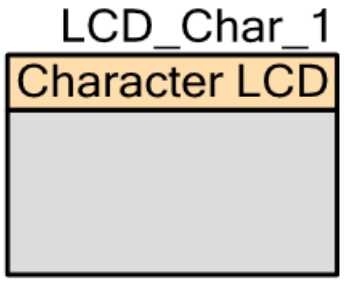
- CAN 2.0A/B spec. compliant
  - Remote Transmission Request (RTR) support
  - Programmable bit rate up to 1Mbps
  - External CAN PHY connects to any GPIO
- Transmit path:
  - 8 transmit message buffers
  - Programmable priority for each
- Receive path:
  - 16 receive message buffers
  - 16 acceptance filters/masks
  - DeviceNet addressing support
  - Option to link multiple receive buffers to/from a hardware FIFO



LCD Drive

Specs:

- Drives up to 736-segments (16-commons/46-front plane)
- Up to 62 total LCD drive pins; commons and segment lines mapped to any GPIO
- High multiplex ratio of up to 1/16 for max 16 segments
- Type A (standard) and Type B (low power) waveforms supported
- Wide operating voltage range supported (2V to 5.2V) for LCD panels
- Static, ½, 1/3, ¼, 1/5 bias voltage levels
- Bias voltage generation using dedicated DAC, and internal resistor leader
- Up to 128 levels of software controlled contrast
- Ability to move display data from memory to LCD via DMA
- Adjustable LCD refresh rate from 10 Hz to 150 Hz



Review

You should now be able to:

- Understand Universal Digital Blocks (UDBs) in PSoC 3 / PSoC 5LP
- Use and implement digital peripherals with PSoC Creator

INTRODUCTION TO PSOC 3 AND PSOC 5LP

DIGITAL PERIPHERALS LAB- LAB 1

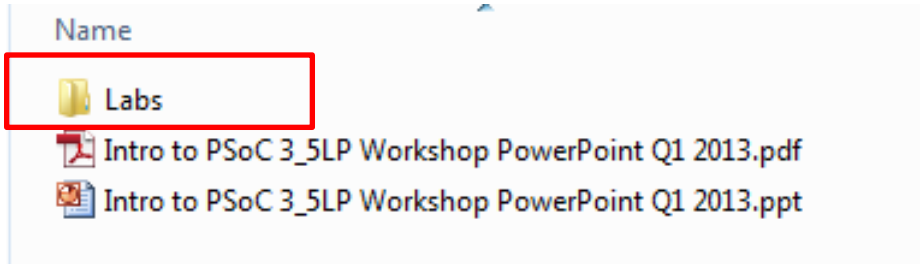
Lab 1

Lab Objective

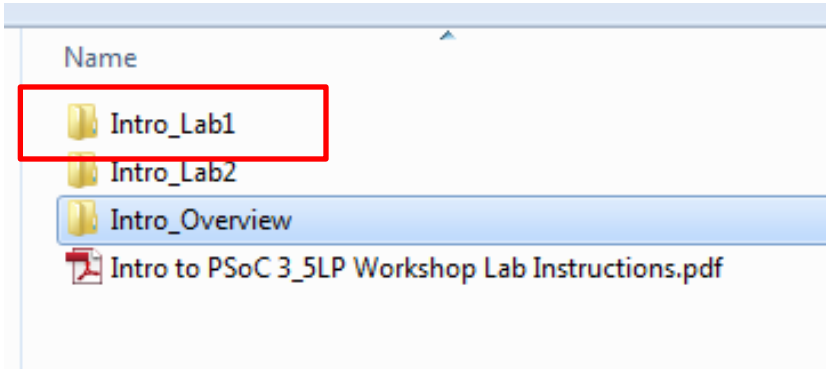
- Make LED3 & LED4 on your PSoC Development Kit blink
- Learn how to place and configure components in PSoC Creator
- Understand the System on Chip Capability of PSoC
- LED3 will blink using two PWMs to change the duty cycle on the LED to make it a “Breathing” LED
- LED4 will blink via software control

Lab 1

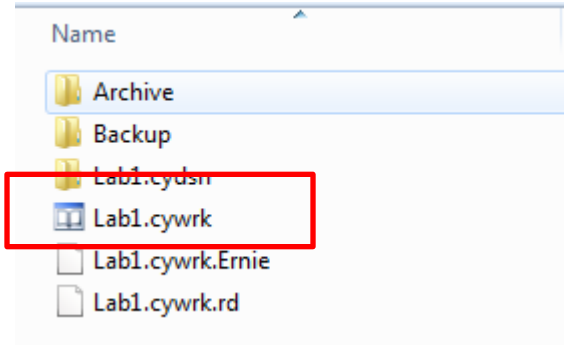
- Open Labs Directory



- Open Intro_Lab1 Directory

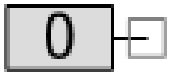
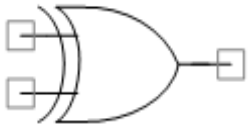
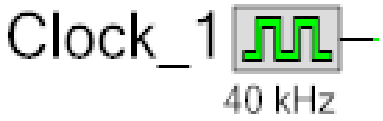
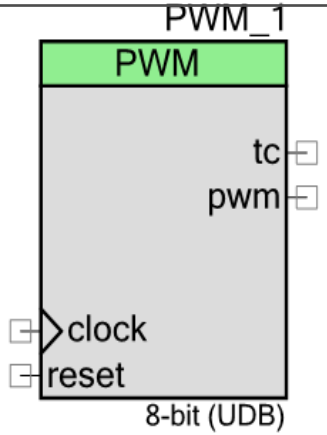


- Double Click ‘Lab1.cywrk’



Lab 1

1. The Software LED has already been configured for you. Follow the instructions below to complete the rest of the design
2. Find the following components found in the Component catalog on the right side of the screen and place them in the boxes given on the “Top Design.cysch” schematic file under Lab_1. Be sure to only place 1 PWM. Components are shown below:

Logic Low ‘0’ 	XOR Gate 
Clock 	PWM 
Digital Output Pin 	

Lab 1

3. Place the components inside the right boxes shown on the schematic file
4. Double click on the clock component to open it in configuration mode and set it to 40 kHz
5. Double click on the PWM component to open it in configuration mode and make the following changes to its properties

Set Properties to:

Implementation: UDB	CMP Value 1: 128
Resolution: 8-Bits	CMP Type 1: Less
PWM mode: One Output	Dead Band : Disabled*
Period: 255	Under Advanced tab:* Interrupts: None

6. Copy the first PWM from the top box into the bottom box and change the "Period" to 254

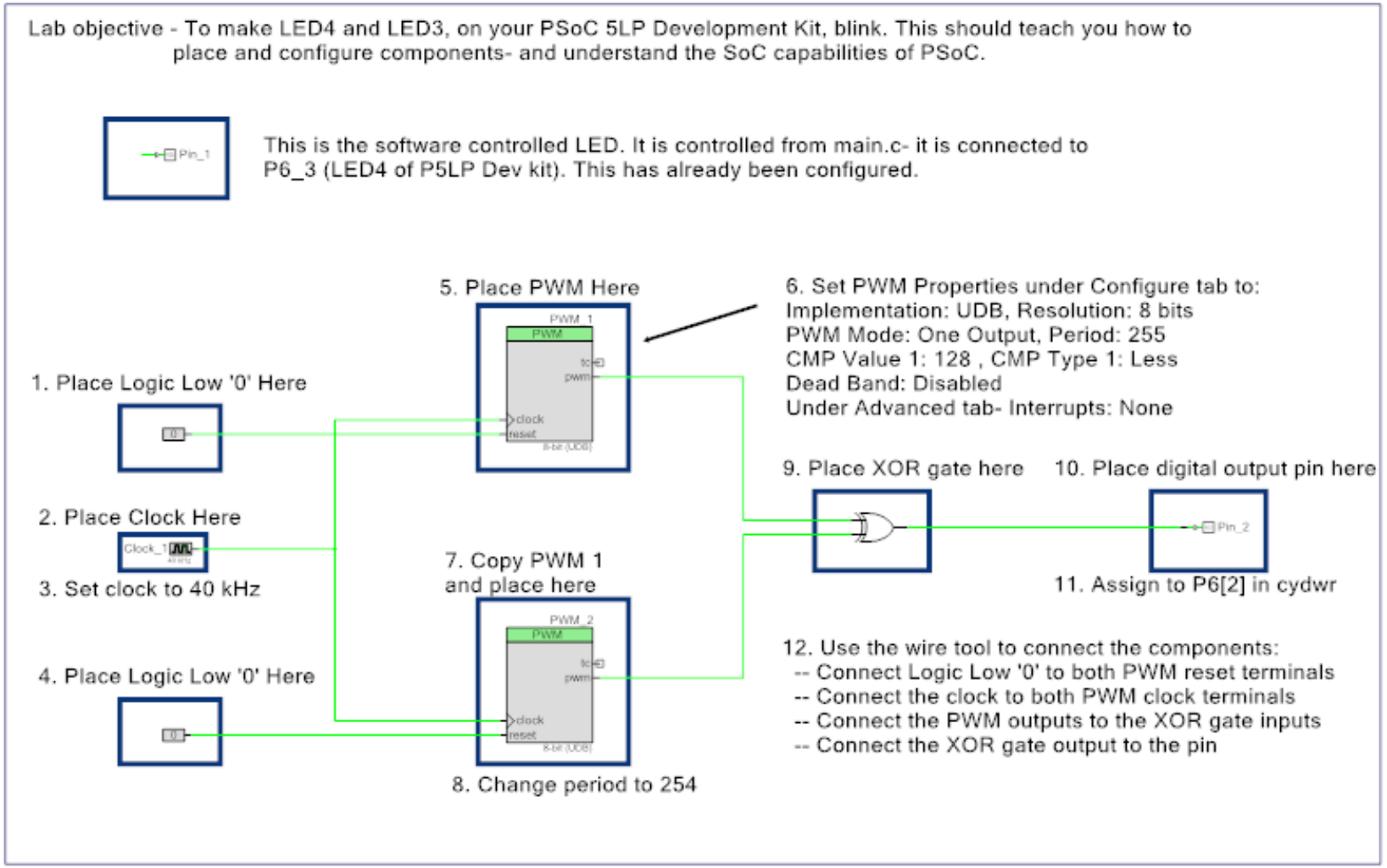
*You may need to expand the customizer window to expose these settings

Lab 1

7. Use the wire tool to make the following connections between the components:
   - Connect Logic Low ‘0’ to PWM reset terminals
   - Connect the clock to both PWM clock terminals
   - Connect the PWM outputs to the XOR gate inputs
   - Connect the XOR gate output to the pin.

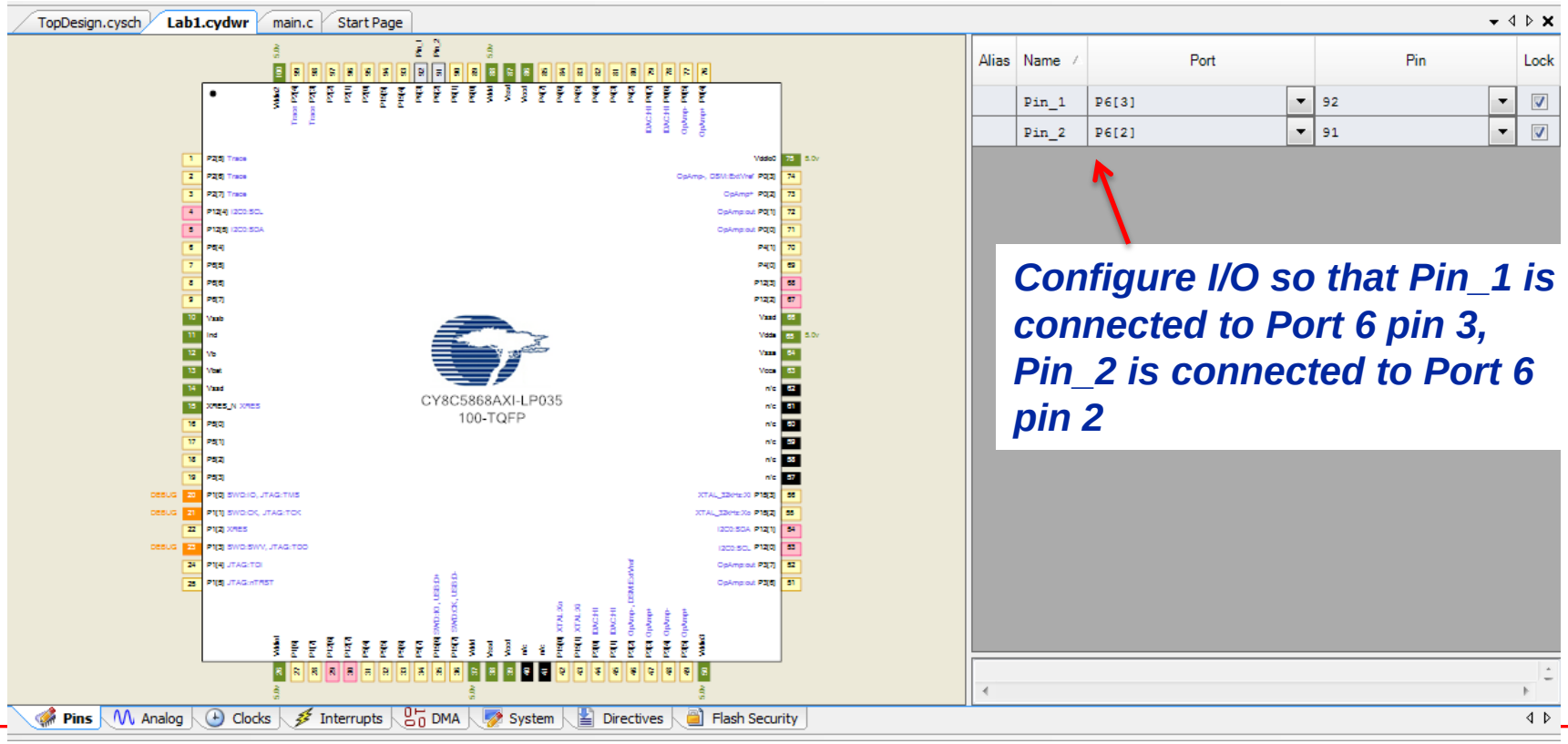
Lab 1

8. Your final schematic should look like this when complete



Lab 1

9. In the Workspace Explorer double click on the .cydwr file to open Design wide Resources
10. In the Design wide Resources tab locate the section for pins on the right
11. Configure the I/O so that Pin 1 is connected to Port 6 pin 3 or P6[3], Pin 2 is connected to Port 6 pin 2 or P6[2]..



Lab 1

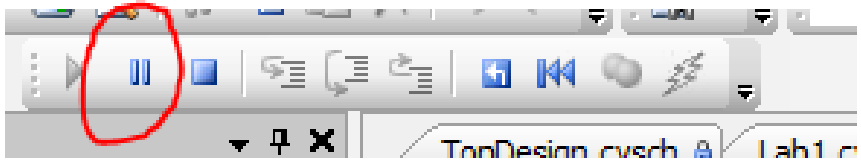
12. Build the project by going to the Build menu selecting Build Digital Peripherals Lab or pressing Shift + F6. This will take some time to build the project.
13. Program the board by going to the Debug menu and in the drop down click Program
14. Push the Reset button on your board located near Port D

    Verify: LED 4 is blinking and LED3 is “Breathing”.

Lab 1

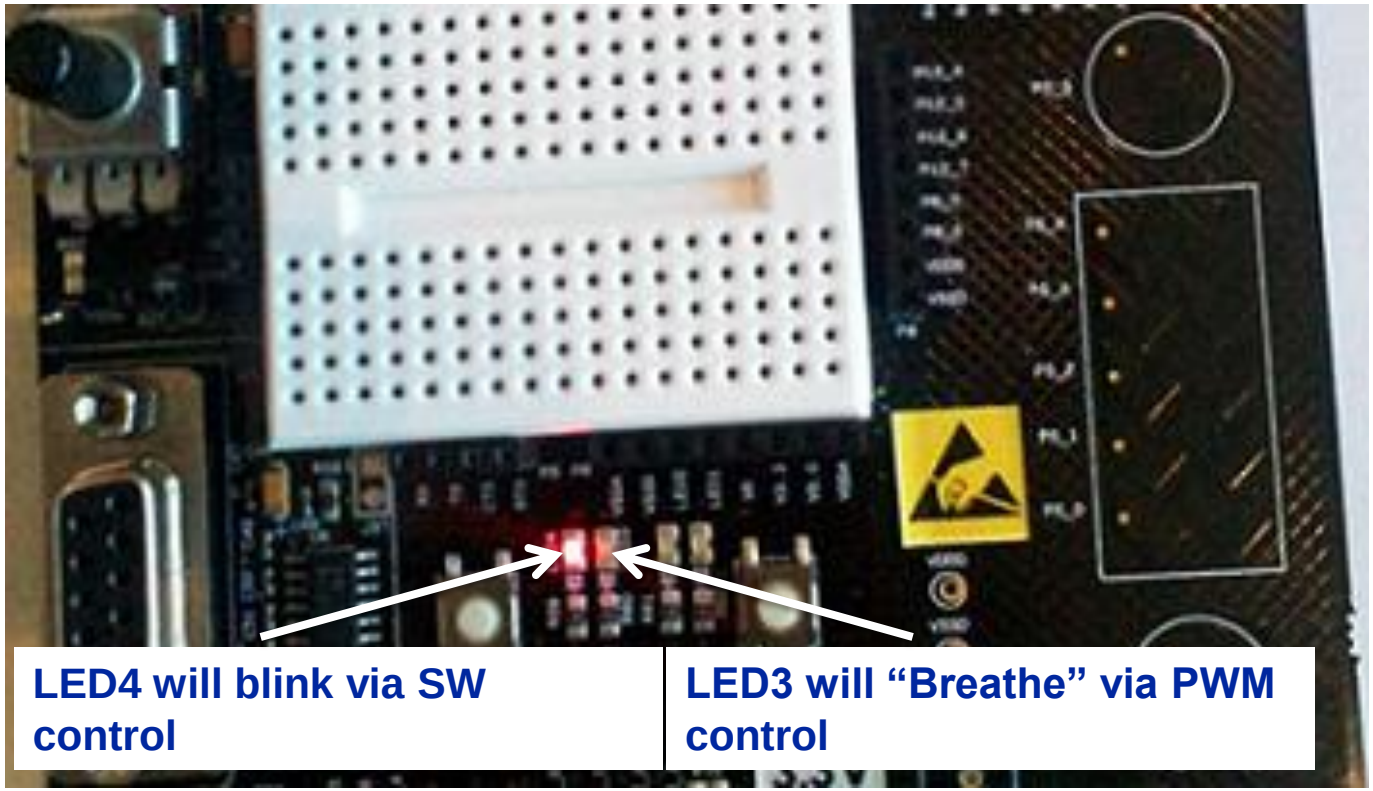
15. Re-program the board by going to the Debug and selecting Debug.
16. Start the program by clicking on the green arrow in the tool bar

17. Allow to run then halt execution-



Validate that LED4 has stopped blinking, LED3 continues to 'Breathe'. Why?

Lab 1


LED4 will blink via SW control
LED3 will “Breathe” via PWM control

INTRODUCTION TO PSOC 3 AND PSOC 5LP

ANALOG PERIPHERALS

Section Objectives

At the end of this section you will be able to

- Understand analog in PSoC 3 / PSoC 5LP
- Use and understand analog peripherals in PSoC Creator

Analog Subsystem

Routing

Multiplexers

Comparators

Opamps

DACs (V & I)

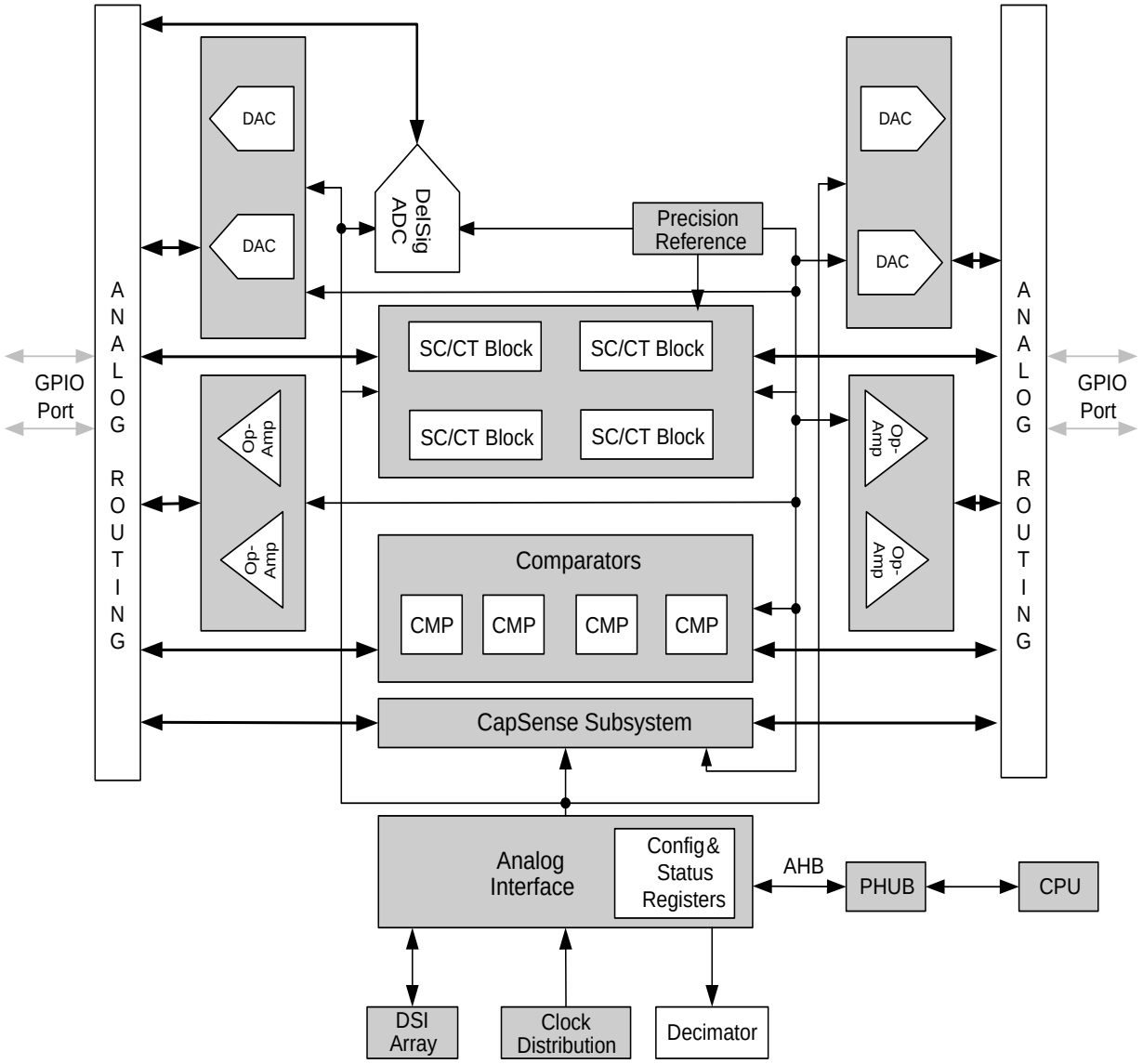
DeltaSigma ADC

Programmable Analog

- PGA
- TIA
- Mixer

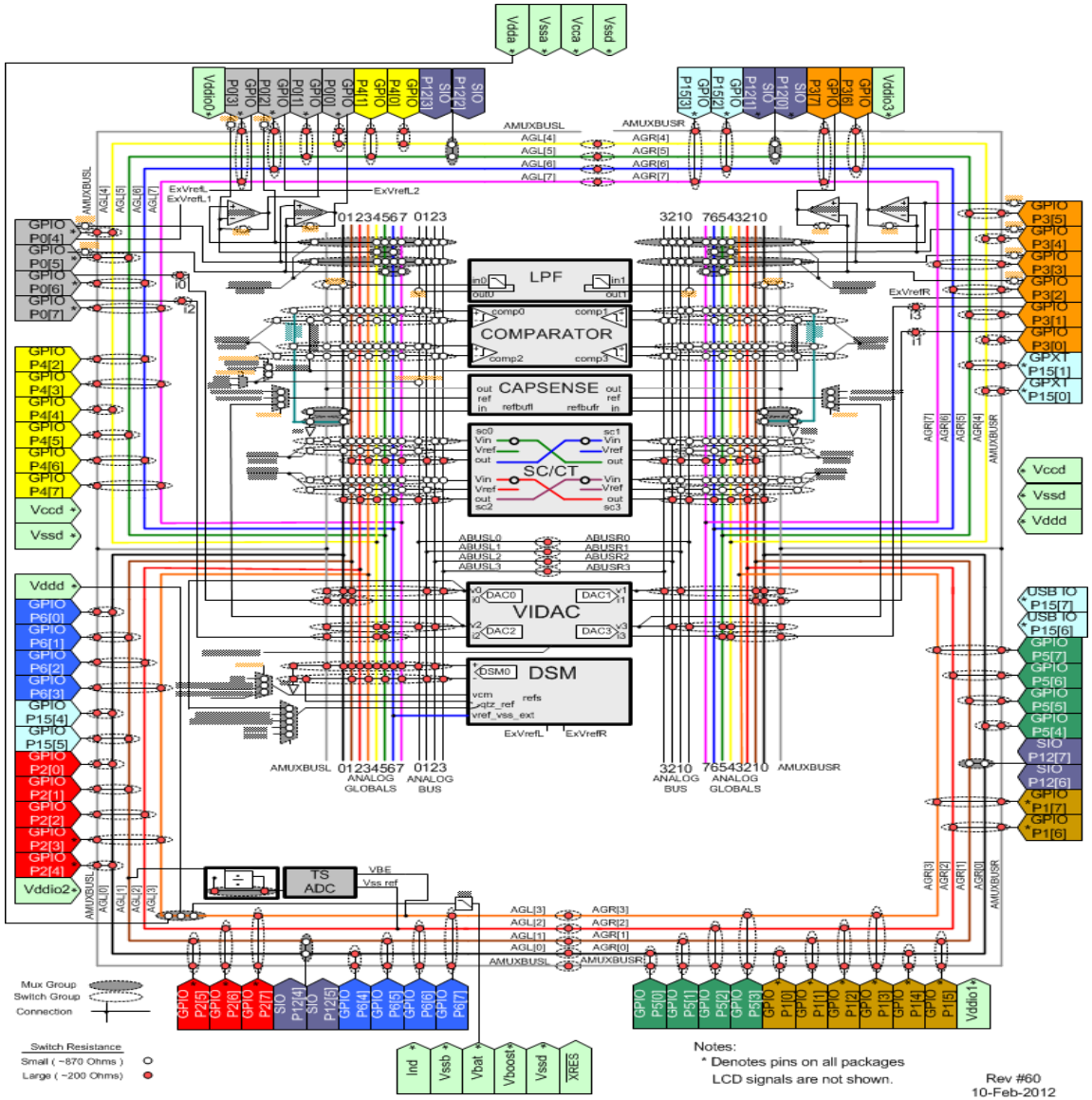
CapSense Touch Sensing

Digital Filters

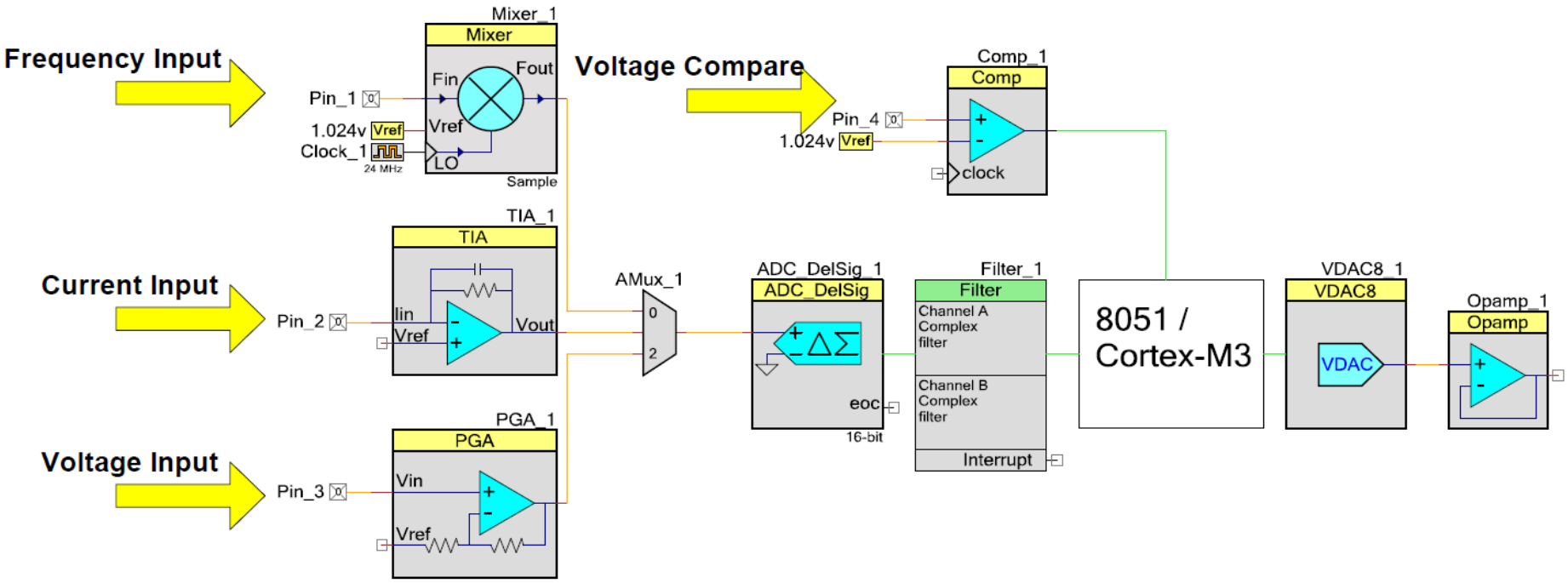


Analog Matrix

More than 320 switches !



Programmable Signal Chain



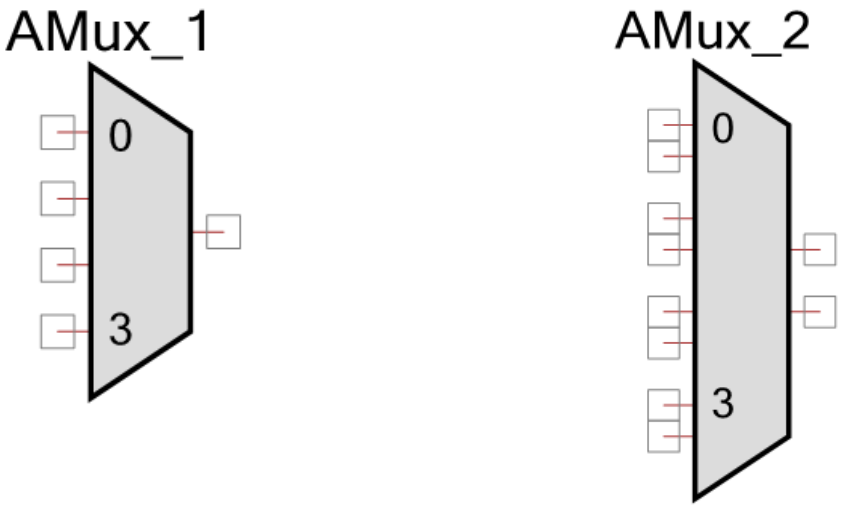
Modern method of signal acquisition, processing, and control with high accuracy, bandwidth and flexibility

- Schematic Entry based design
- Automatic place and route
- Optimizations for analog and digital routing

Routing with Muxes

Analog Multiplexer Specs:

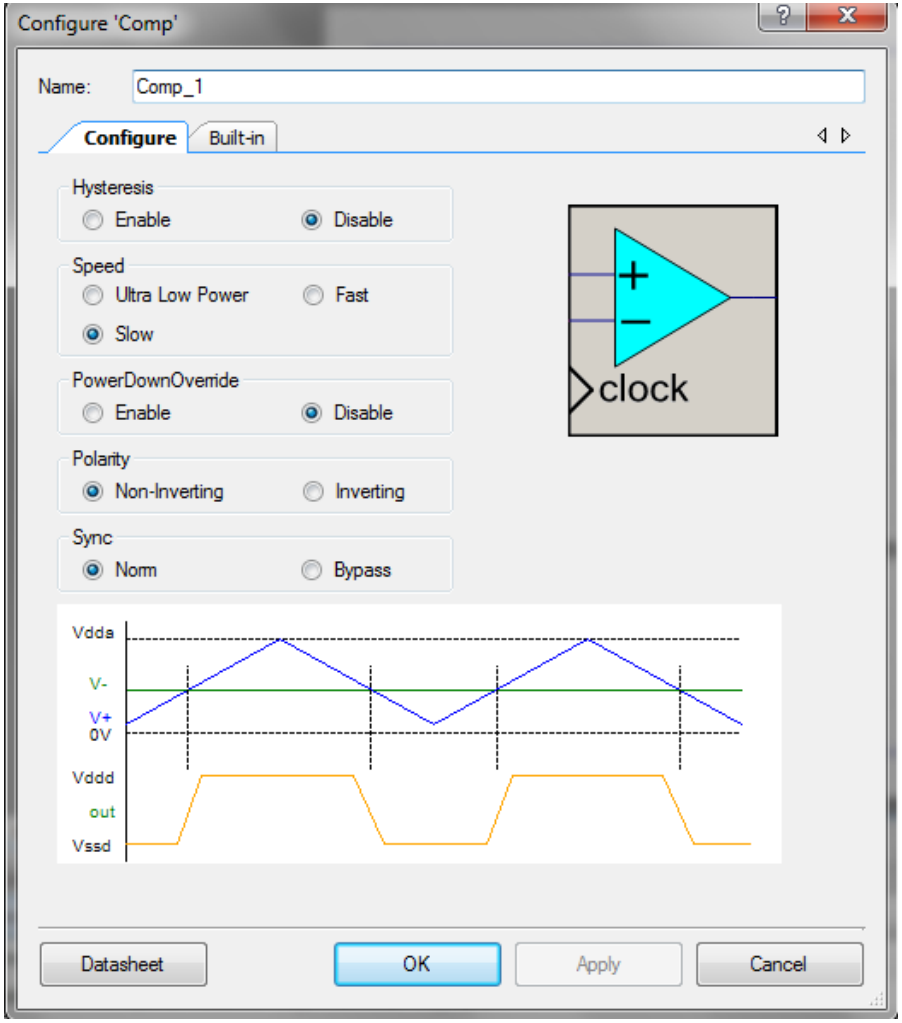
- Bi-directional
- Either single ended or differential
- Actual routing hidden from user
- May have more than one connection at a time
- Analog routing may be controlled by digital subsystem



Analog Peripheral: Comparator

Specs:

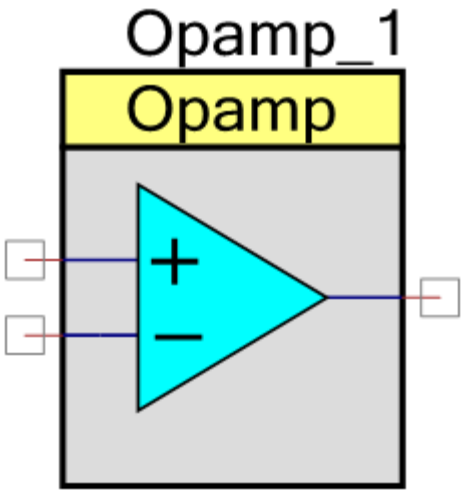
- Up to four per device
- Speeds:
  - Fast – 80 ns / 250 uA
  - Slow – 55 us / 6 uA
- Accuracy:
  - 2 mV fast mode
  - Zero-adjust; Internal VDAC
- Hysteresis:
  - 10 mV nominal
  - May be enabled or disabled



Analog Peripheral: Opamp

Specs:

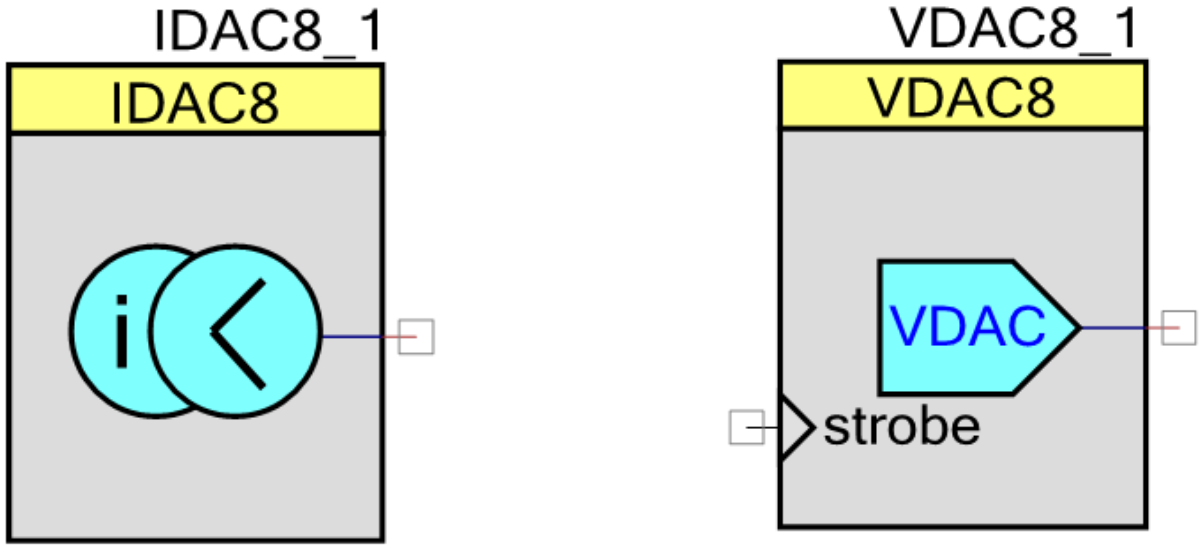
- Follower or Opamp configuration
- Unity gain bandwidth > 3.0 MHz
- Input offset voltage 2.0 mV max
- Rail-to-rail inputs and output
- Output direct low resistance connection to pin
- 25 mA output current
- Programmable power and bandwidth
- Internal connection for follower (saves pin)



Analog Peripheral: VDAC8 and IDAC8

Features

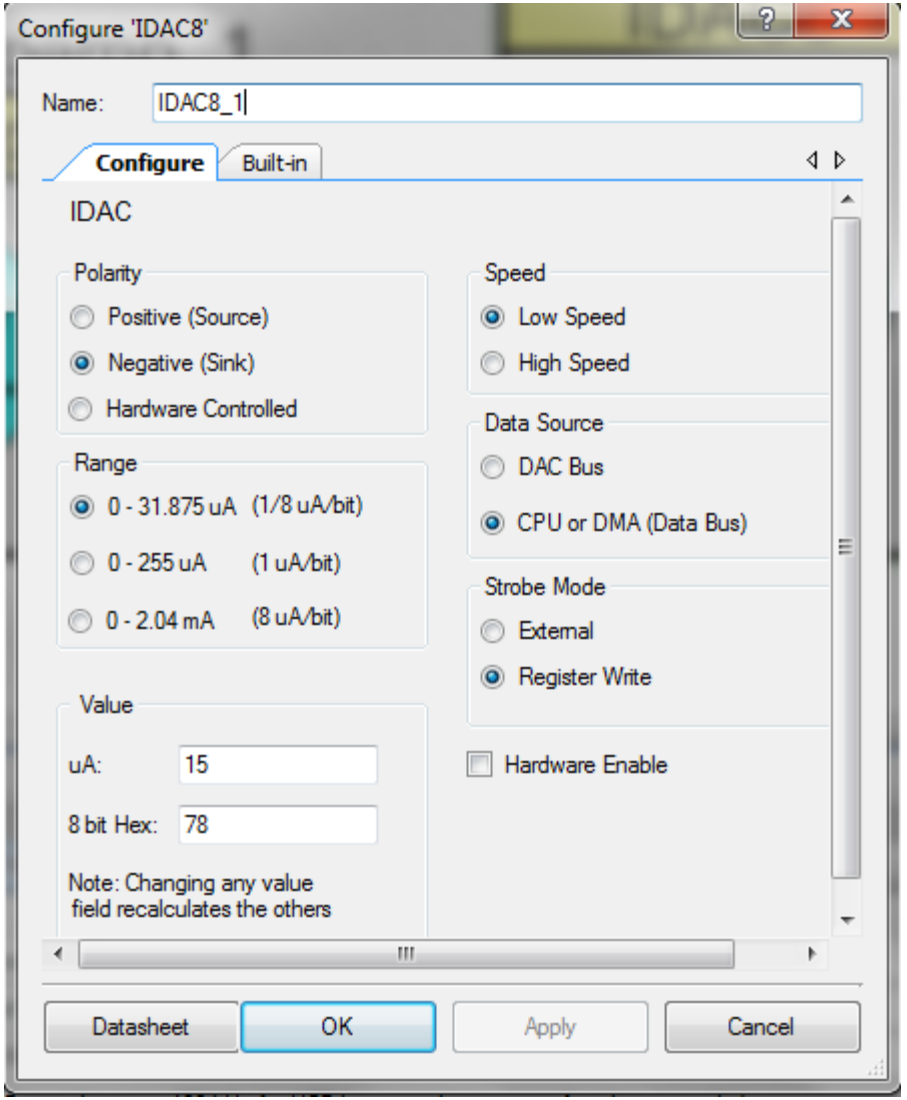
- DAC data source may be data register or DAC Bus
- CPU or DMA may write to data register
- Data Strobe from data register write or Strobe input
- Clock or UDB may be used for Strobe
- IDAC8 and VDAC8 are the same block with V and I inputs



Analog Peripheral: IDAC8

Specs:

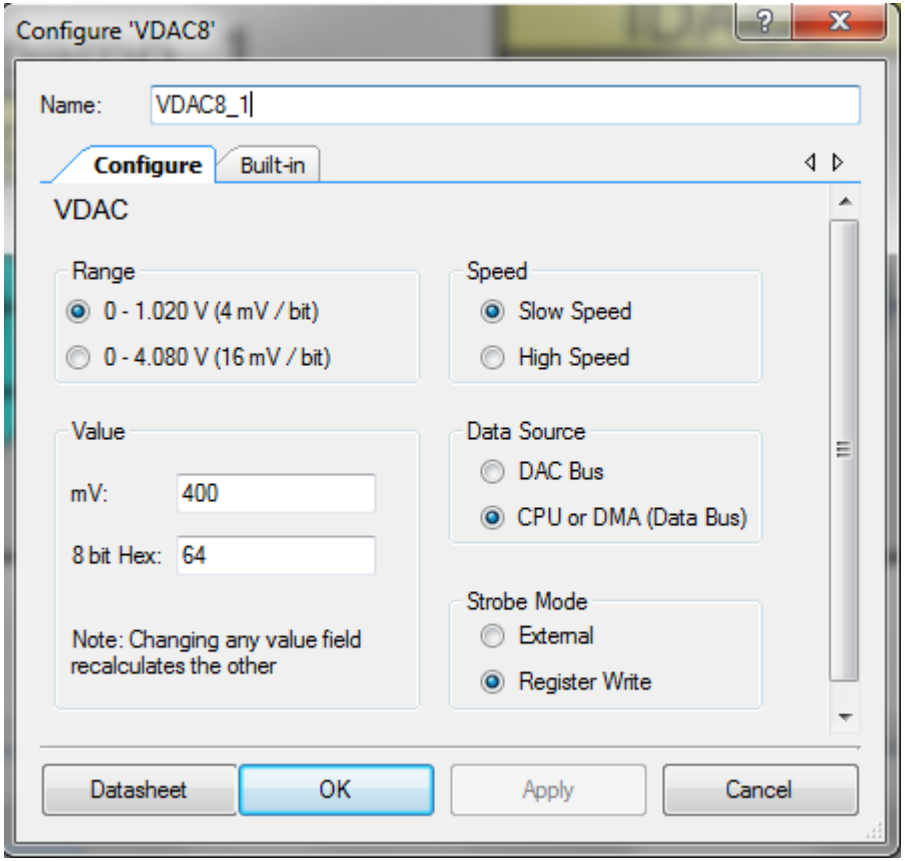
- Source or sink
- Ranges:
  - 0 to 31.875 uA (125 nA/bit)
  - 0 to 255 uA (1 uA/bit)
  - 0 to 2.04 mA (8 uA/bit)
- Power (ICC):
  - 100 uA max slow mode
  - 500 uA max fast mode



Analog Peripheral: VDAC8

Specs:

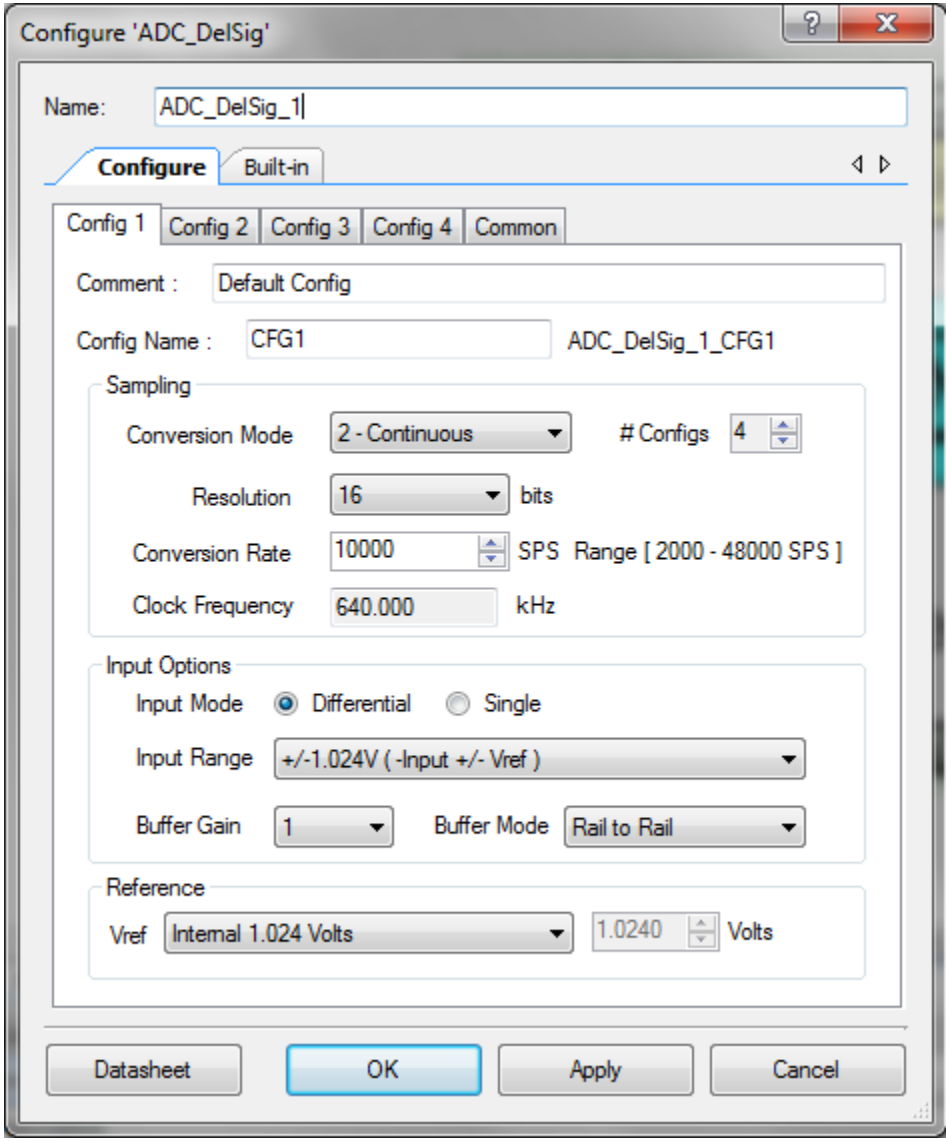
- Ranges:
  - 0 to 1.02V (4mV/bit)
  - 0 to 4.08V (16mV/bit)
- Output R = ~16 k ohms (4 volt range)
  - Must be buffered for external use
  - Some internal loads don't require buffering
- Power (ICC):
  - 100 uA max slow mode
  - 500 uA max fast mode
- Speed:
  - 1 Msps (1V mode)
  - 250 ksps (4V mode)



Analog Peripheral: Delta Sigma ADC

Specs:

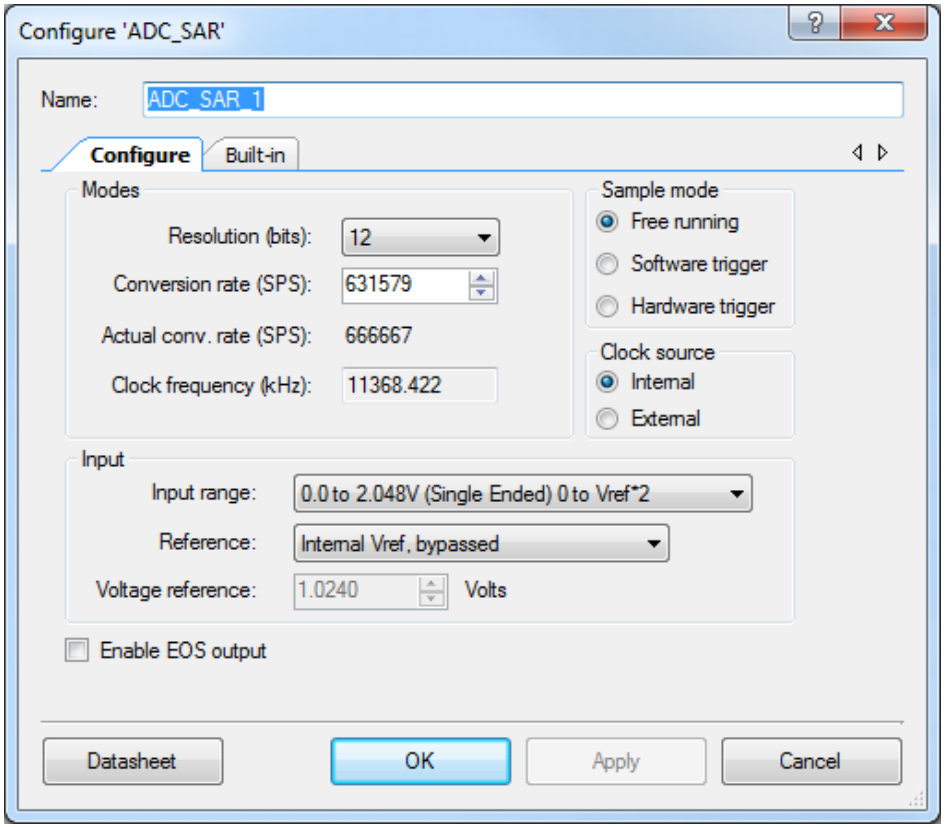
- High speed, high resolution ADC
- Selectable resolutions (8- to 20-bit)
- Several input ranges
- High-impedance input buffers
  - Programmable gain (1,2,4,8)
  - Chopper mode for low offset
  - Internal reference may be bypassed
- Single and differential input modes
- Wide range of sample rates 10 to 375K
- Multiple reference sources
- Drop, connect, and go!



Analog Peripheral: SARADC

Specs:

- High speed ADC (up to 1 Msps)
- Selectable resolutions (8- to 12-bit)
- Several input ranges
- Single and differential input modes
- Low SNR (57 dB SINAD)
- Low Distortion (0.1 THD)
- Four Power Modes
- Multiple reference sources
- Drop, connect, and go!
- Typical Applications
  - LED lighting control
  - Motor Control
  - Magnetic Card Reader
  - High-Speed data collection
  - Power Meter, Pulse Oximeter, more!



Programmable Analog Peripherals

Specs:

- Combination of functions from PSoC1 programmable analog catalog
- Switched-Capacitor (SC)-based analog
- Continuous Time blocks (CT)-based analog

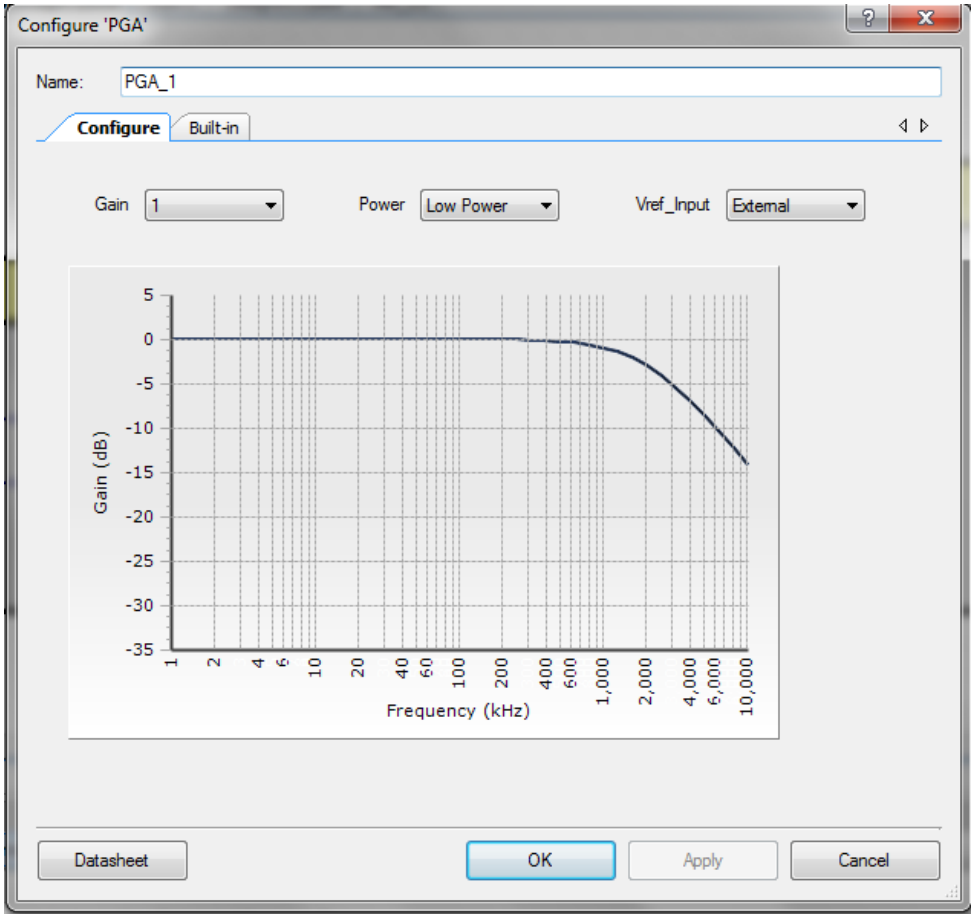
Analog Peripheral: PGA

Specs:

- Programmable Gain Amplifier
- Amplify signals without external components
- Gain: 1x to 50x
- Vin and Vref to any pin

Accuracy:

- Gain: +/- 5%
- Vos: 10 mV



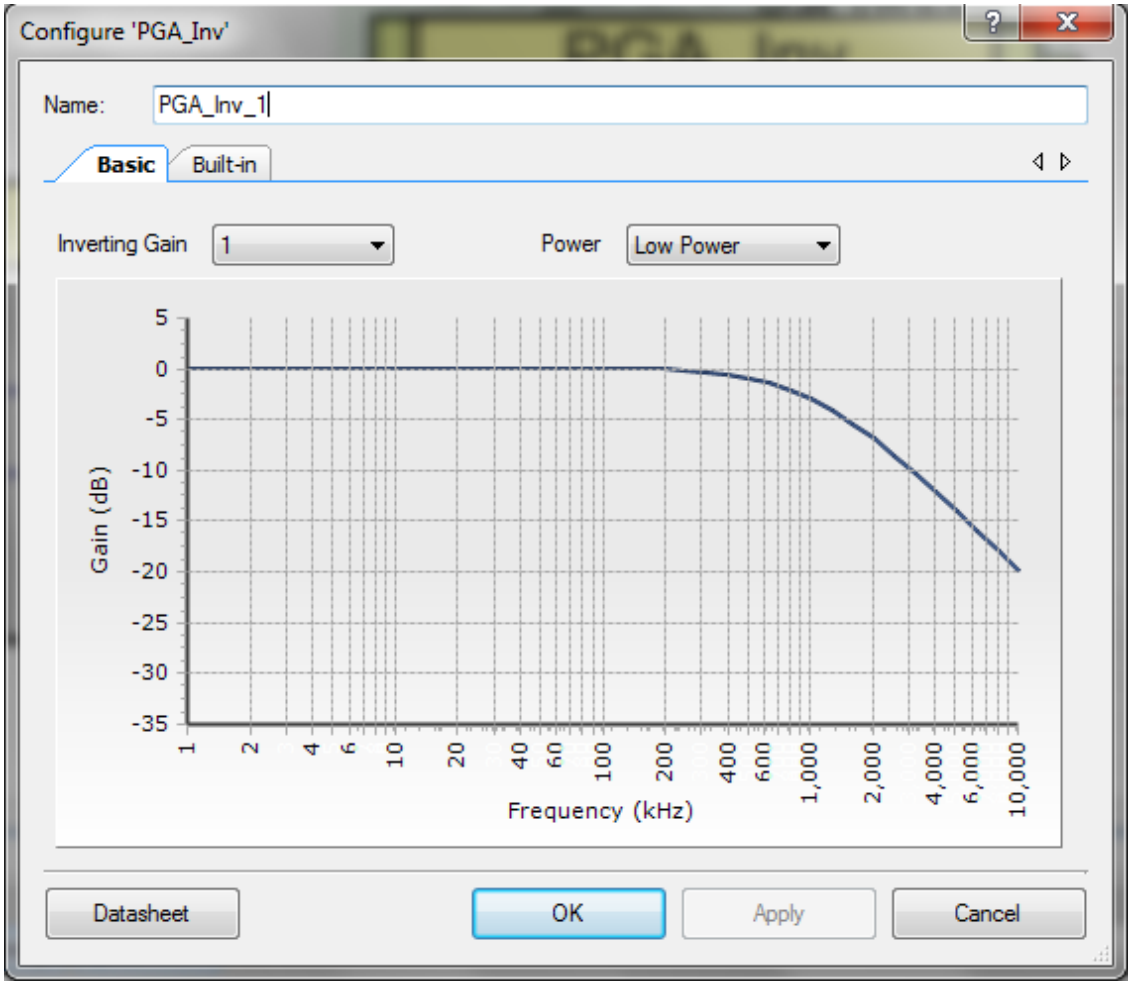
Analog Peripheral: PGA_Inv

Specs:

- Inverting PGA
- Amplify signals without external components
- Gain: -1x to -49x
- Vin and Vref to any pin

Accuracy:

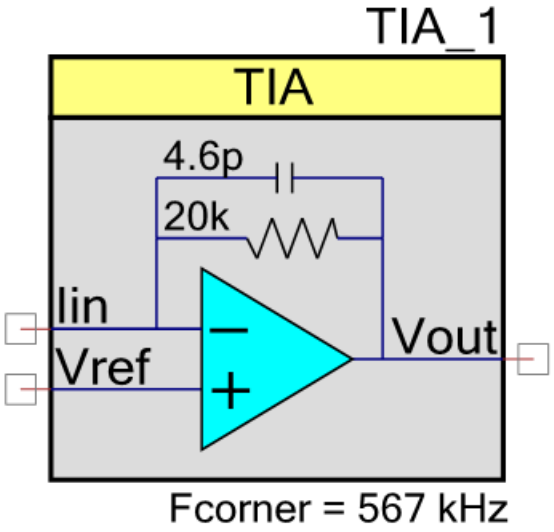
- Gain: +/- 5%
- Vos: 10 mV



Analog Peripheral: TIA

Specs:

- Trans-Impedance Amplifier
- Conversion gain is a “resistor”
  - Current IN -> Volts OUT
  - Vout = Vref – Iin*Rfb
  - Adjustable Rfb = Programmable gain (20k to 1M)
  - Adjustable Cfb = Programmable bandwidth (up to 4.7 pF)
  - Calibrated with on-chip IDAC (internal resistors +/- 30%)
- Applicable to current output sensors
  - Glucose meters
  - Photo-diodes – light meters, medium speed IR receiver



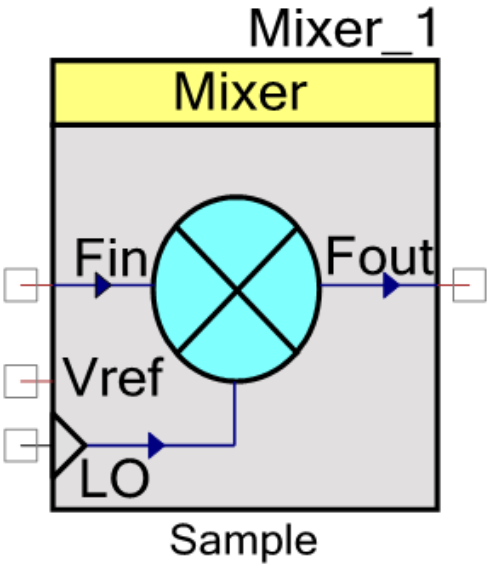
Analog Peripheral: Mixer

Specs:

- LO_Freq = Local Oscillator

Mixer Modes:

- Up-Mixer: Multiplier
  - Clock up to 1.0 MHz
  - Output at LO_Freq +/- Fin
  - Example 200 kHz input clocked at 255 kHz to narrowband filter at 455 kHZ

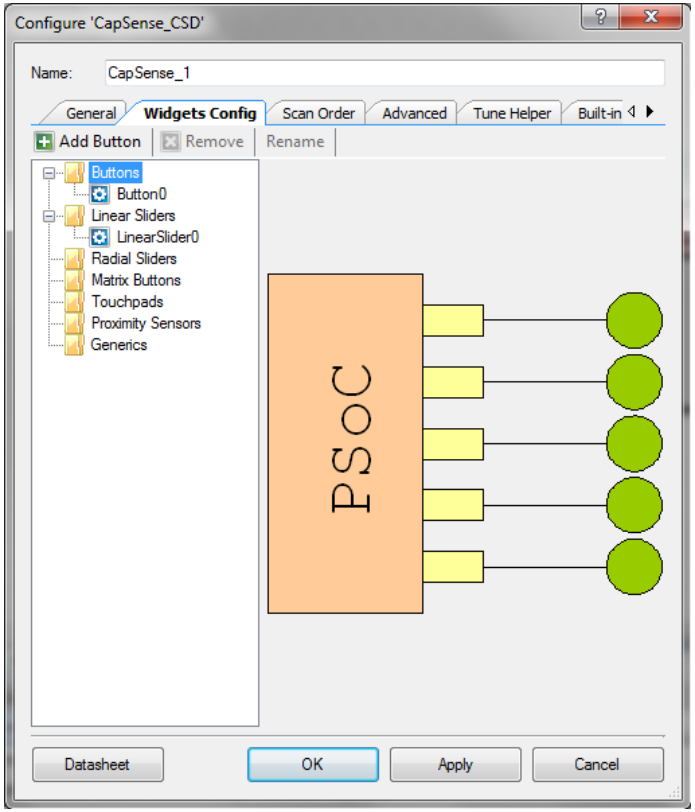


- Down-Mixer Sampler
  - Clock up to 4.0 MHz
  - Output at Fin – LO_Freq
  - Example 455 clocked at 435 kHz to low-pass filter at 25 kHz

Analog Peripheral: CapSense®

Specs:

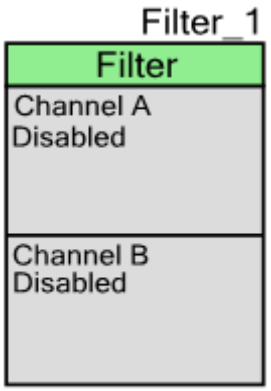
- CapSense peripheral uses configuration of existing system resources
- Two simultaneous CapSense systems possible
- CapSense Configurations
  - All have similar configuration patterns
  - Buttons: Basic CapSense sensor with On/Off detection
  - Sliders: Linear and radial with interpolated positioning (also supports diplexing to reduce pin count)
  - Touch Pads: X, Y interpolated positioning
  - Matrix Buttons
  - Proximity Sensors
  - Generic Sensors

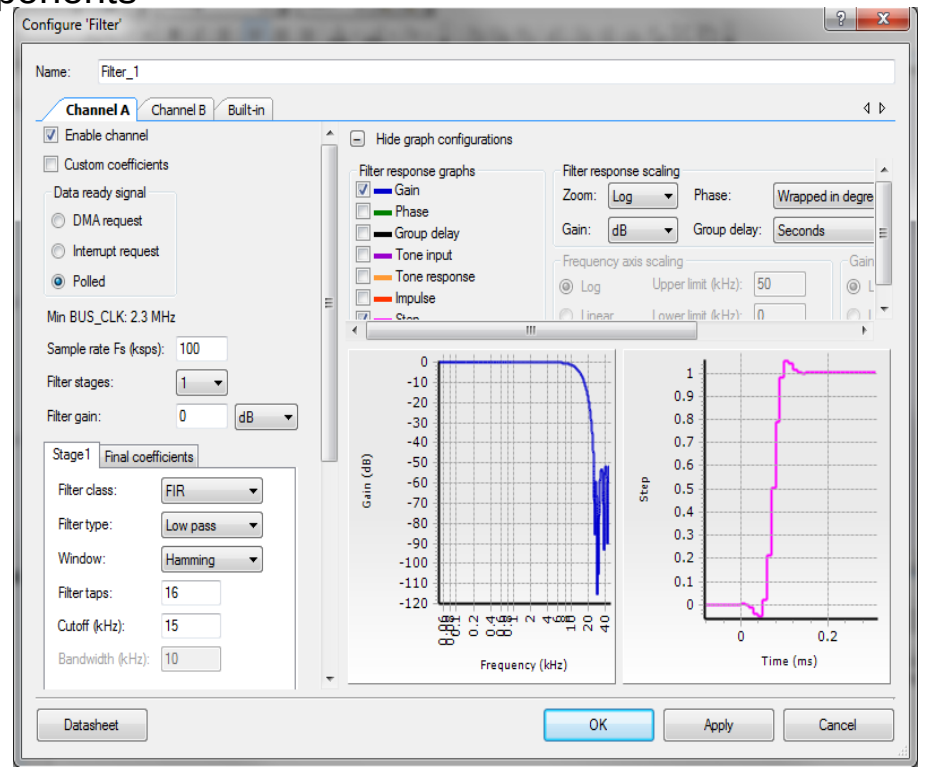


Analog Peripheral: DFB

Specs:

- Digital Filter Block
- What it does:
  - Works on digitized data from ADC or any other source
  - Sequentially calculate multiple filters
  - Removes noise and unwanted frequencies from signals
  - Replaces analog filters requiring external components
- How it works:
  - No coding or coefficients! All handled by GUI
  - 24-bit filter co-processor
  - 128 pairs of data/coefficients
- Setting for filters can be made for 2 channels
- Select type:
  - Low Pass, Band Pass, High Pass, Notch
- Select implementation:
  - FIR or IIR Biquad
- Specify sample rate
- Specify number of taps
- Select frequency parameters





Review

You should now be able to:

- Understand analog in PSoC 3 / PSoC 5LP
- Use and understand analog peripherals in PSoC Creator

INTRODUCTION TO PSOC 3 AND PSOC 5LP

ANALOG PERIPHERALS LAB- LAB 2

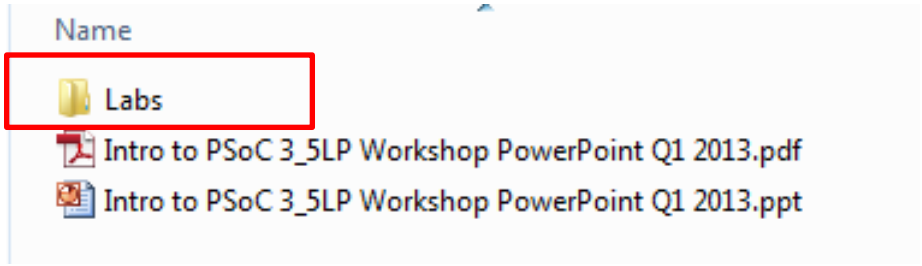
Lab 2

Lab Objective

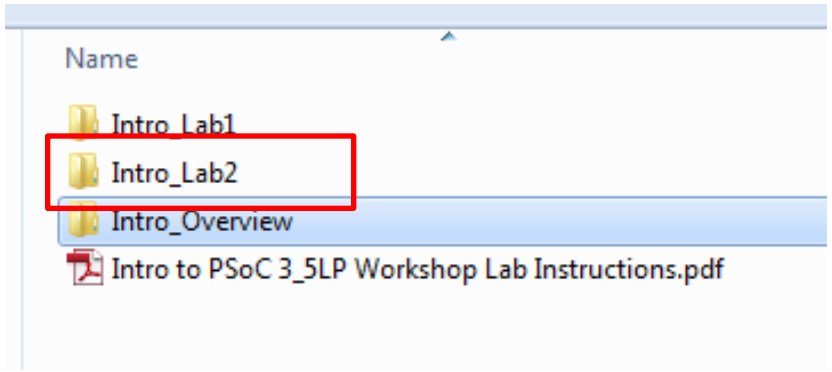
- To convert an output from the potentiometer into a digital number using the ADC
- To display the digital number on the LCD Screen on PSoC Development Kit

Lab 2

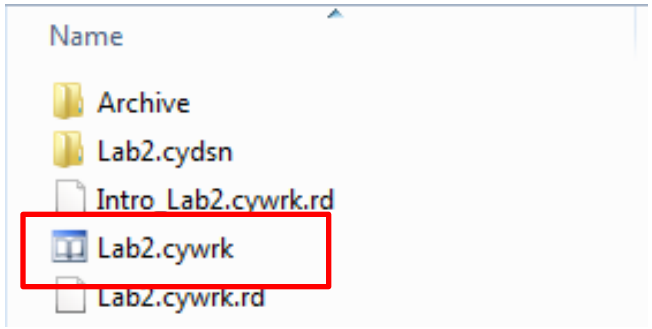
- Open Labs Directory



- Open Intro_Lab2 Directory



- Double Click ‘Lab2.cywrk’



Lab 2

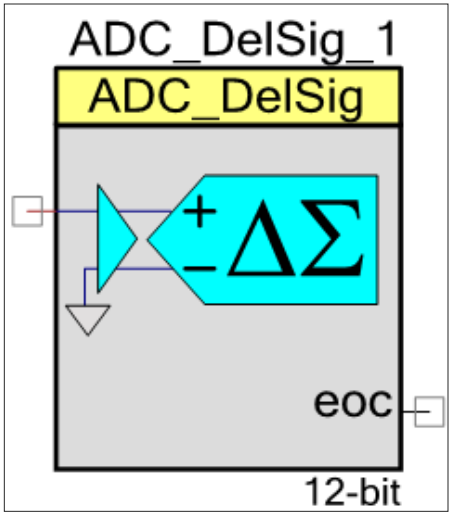
Instructions:

1. Place the Analog Pin from Component Catalog as shown here in the adjacent box

2. Place the Delta Sigma ADC in the box as shown below.
3. Double-click on the component to open it in the configuration mode and make the following changes:

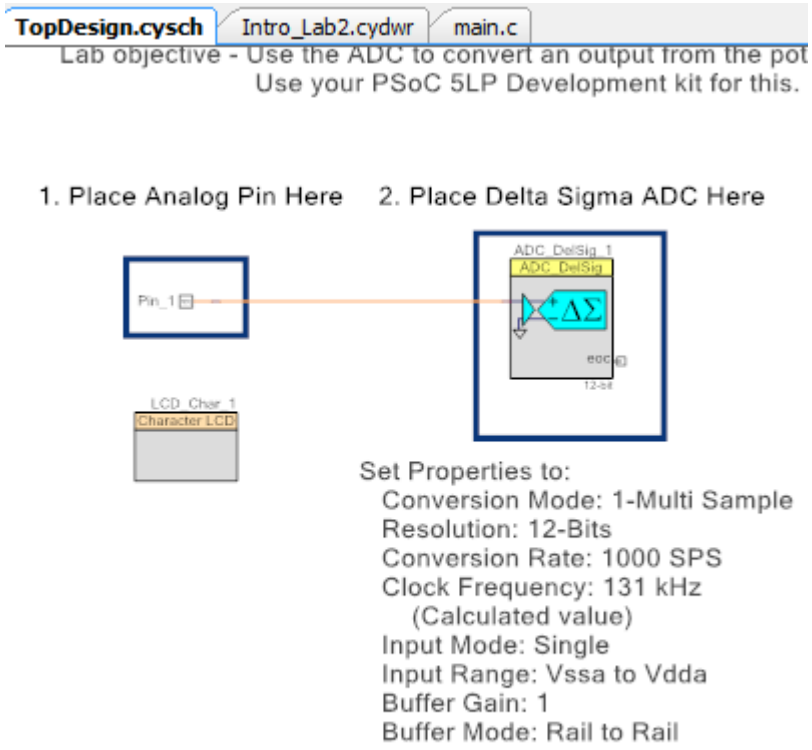
Set Properties to:

Conversion Mode: 1-Multi Sample	Input Mode: Single
Resolution: 12-Bits	Input Range: Vssa to Vdda
Conversion Rate: 1000 SPS	Buffer Gain: 1
Clock Frequency: 131 kHz (Calculated value)	Buffer Mode: Rail to Rail



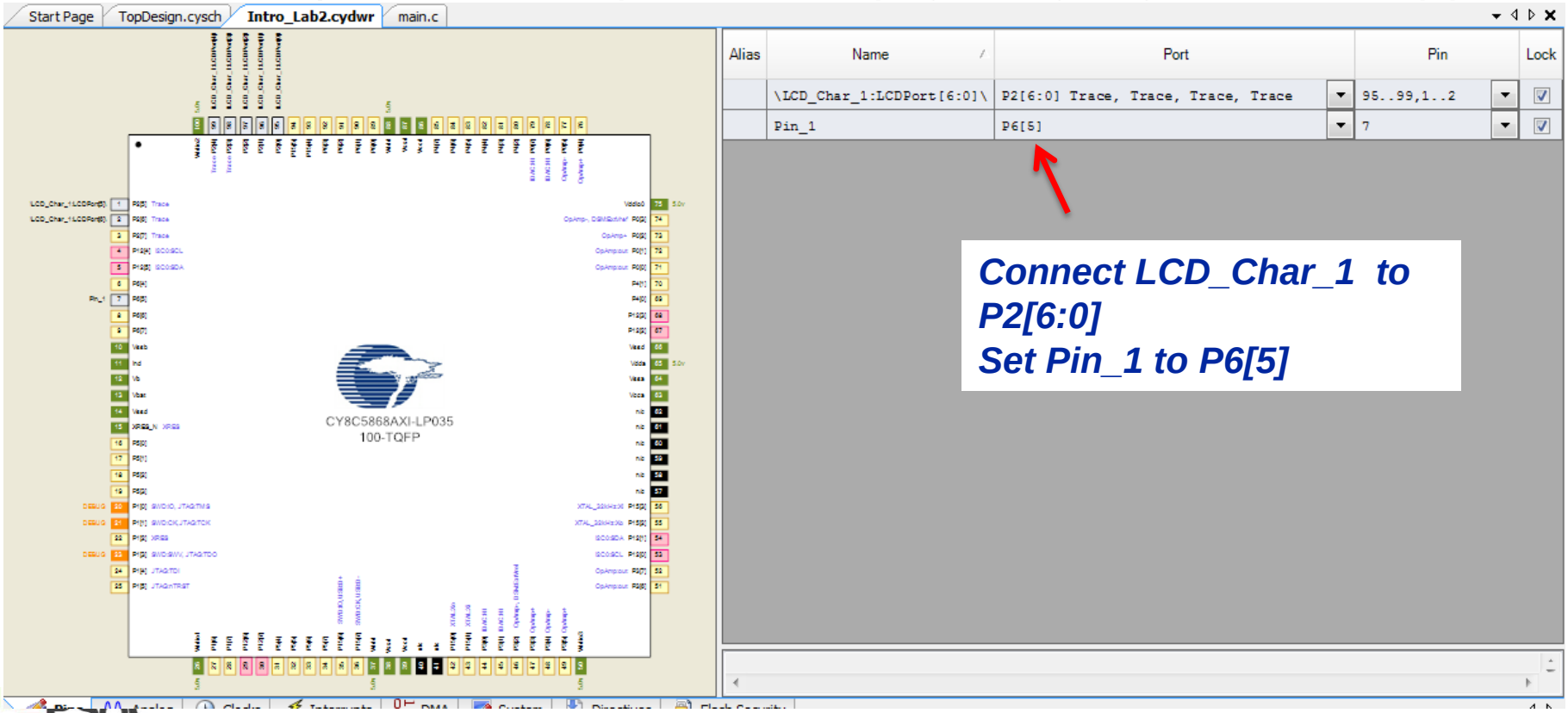
Lab 2

4. Use the wire tool found on the left side of the worksheet (shown in slide 23) to connect Pin 1 to the ADC input. To use the wire tool hover over the connections until an ‘X’ appears, then click to make the connection.
5. Your final schematic should look like this when complete



Lab 2

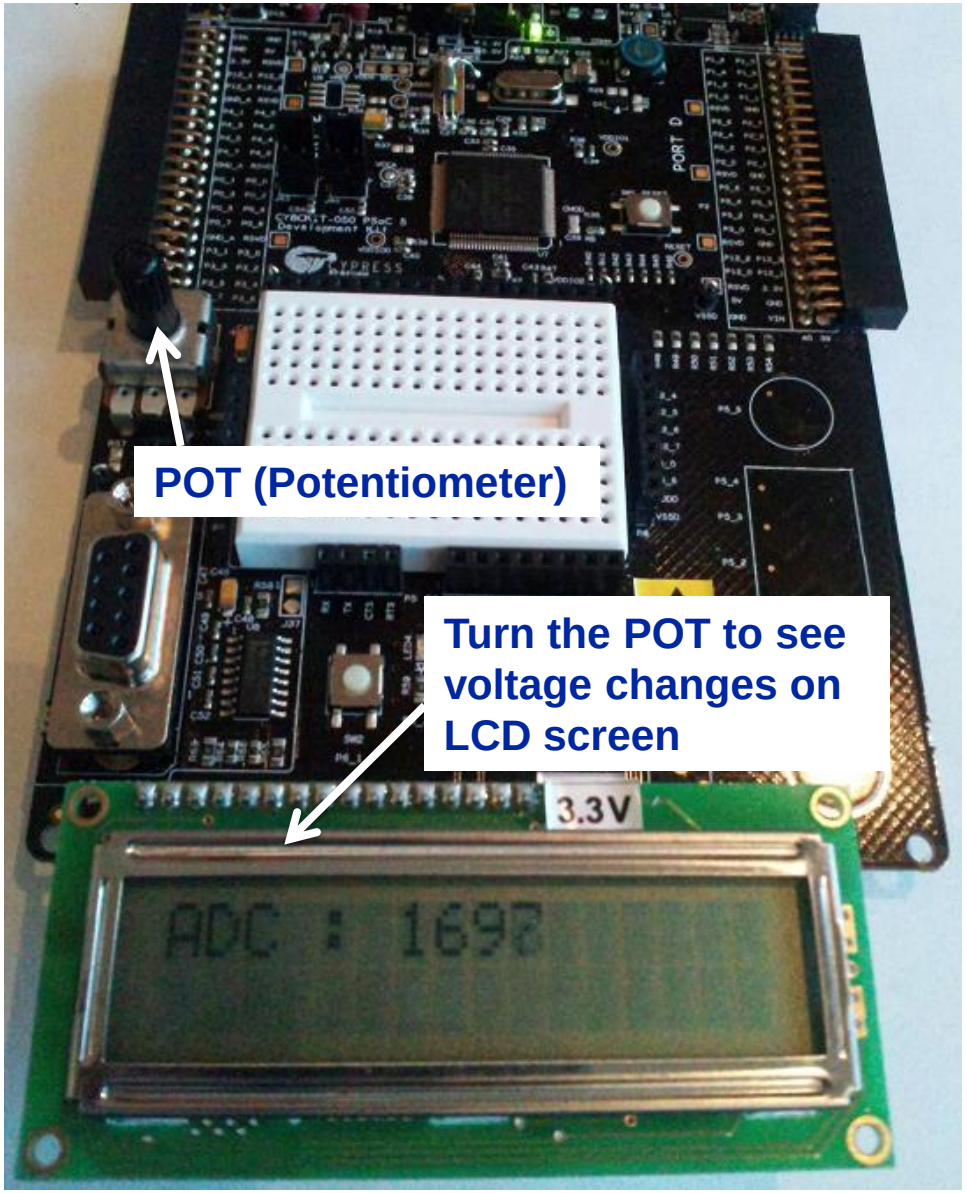
6. In the Workspace Explorer double click on the .cydwr file to open Design wide Resources (as explained in Overview lab)
7. In the Design wide Resources tab locate the section for pins on the right
8. Connect the LCD to Port 2 by assigning LCDPort[6:0] to P2[6:0]. Connect Pin 1 to the potentiometer (Port 6, Pin 5) by assigning Pin_1 to P6(5).



Lab 2

9. Build the project by going to the Build menu selecting Build System Resources Lab. This will take some time to build the project.
10. At this point, verify that the board is plugged in.
11. Program the board by going to the Debug menu and in the drop down click Program
12. Push the Reset button on your board located near Port D
13. Verify: When you turn the POT you should see the ADC values change

Lab 2


POT (Potentiometer)
Turn the POT to see voltage changes on LCD screen
3.3V
ADC : 1698

Review

Topic	Objective
PSoC3/5LP Architecture Overview	Understand the CPU, Digital, Analog and Programmable Routing and Interconnect Subsystems
System Resources	Understand the system block diagram of PSoC 3 / PSoC 5LP devices
Digital Peripherals	Understand Universal Digital Blocks (UDBs) in PSoC 3 / PSoC 5LP
Analog Peripherals	Understand analog in PSoC 3 / PSoC 5LP

Free Kit Upgrade Program

Free kit upgrade program is applicable for customers with kits based on PSoC 5 silicon

3 Simple Steps to Upgrade Kits

1. Log on to www.cypress.com/go/psockitupgrade
2. Fill in your kit details (board Id #) and receive an email with the promo-code
   Board Id# is 11 character long and is located at the back of the board and kit box
3. Shop for your kit and add promo-code on checkout

This process is available on the PSoC 5 web page

CY8CKIT-050 PSoC 5LP Development Kit

CY8CKIT-010 CY8C58LP Family Processor Module Kit

Next Steps

www.cypress.com/support & www.cypress.com/psoc

- PSoC 3 & PSoC 5LP Kits and Expansion Board Kits
- PSoC Developer Community
- Online Trainings
- Application Notes
- Technical Support